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1. GENERAL DESCRIPTION

The W19B320BT/B is a 32Mbit, 2.7~3.6-volt single bank CMOS flash memory organized as 4M x 8 or 2M × 16 bits. The word-wide (× 16) data appears on DQ15-DQ0, and byte-wide (x 8) data appears on DQ7-DQ0. The device can be programmed and erased in-system with a standard 3.0-volt power supply. A 12-volt VPP is not required. The unique cell architecture of the W19B320BT/B results in fast program/erase operations with extremely low current consumption (compared to other comparable 3-volt flash memory products). The device can also be programmed and erased by using standard EPROM programmers.

2. FEATURES

Performance

- 2.7~3.6-volt write (program and erase) operations
- Fast write operation
  - Sector erases time: 0.4 Sec (typical)
  - Chip erases time: 30Sec (typical)
  - Byte/Word programming time: 7/9 s (typical)
- Read access time: 70 ns
- Typical program/erase cycles: 100K
- Twenty-year data retention
- Ultra low power consumption
  - Active current (Read): 10 mA (typical)
  - Active current (Read while Erase): 21 mA (typical)
  - Standby current: 0.2 μA (typical)

Architecture

- Sector erase architecture
  - Eight 8KB, and sixty-three 64KB sectors
  - Top or bottom boot block configurations available
  - Supports full chip erase
- Security Sector Size: 256 Bytes
  - The Security Sector is an OTP; once the sector is programmed, it cannot be erased
- JEDEC standard byte-wide and word-wide pinouts
- Manufactured on WinStack 0.13μm process technology
- Available packages: 48-pin TSOP and 48-ball TFBGA (6x8mm)

Software Features

- Compatible with common Flash Memory Interface (CFI) specification
  - Flash device parameters stored directly on the device
  - Allows software driver to identify and use a variety of different current and future Flash products
- Erase Suspend/Erase Resume
  - Suspends erase operations to allow programming in same bank
- End of program detection
  - Software method: Toggle bit/Data polling
- Unlock Bypass Program command
  - Reduces overall programming time when issuing multiple program command sequences

Hardware Features

- Ready/#Busy output (RY/#BY)
  - Detect program or erase cycle completion
- Hardware reset pin (#RESET)
  - Reset the internal state machine to the read mode
- #WP/ACC input pin
  - Write protect (#WP) function allows protection of two outermost boot sectors, regardless of sector protection status

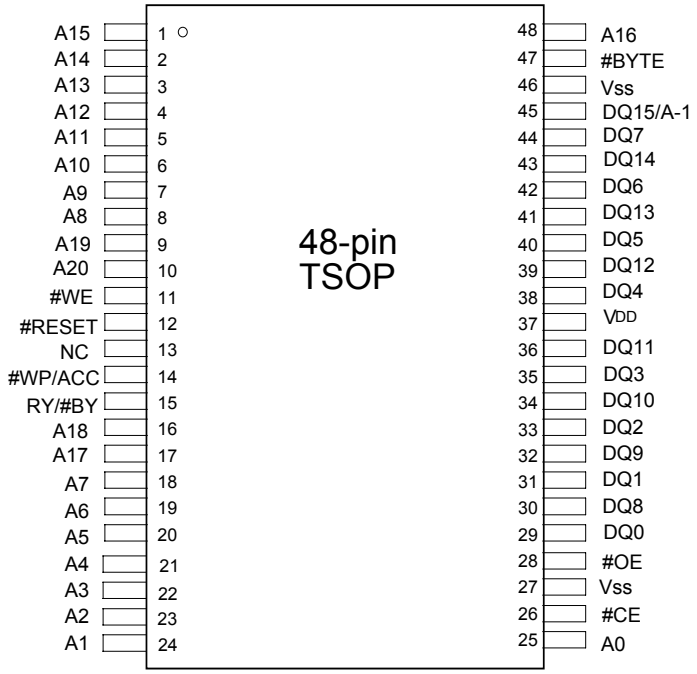
Temperature range

- Extended temperature range (-20℃ to 85 ℃)
- Industrial devices ambient temperature(-40℃ to +85℃)

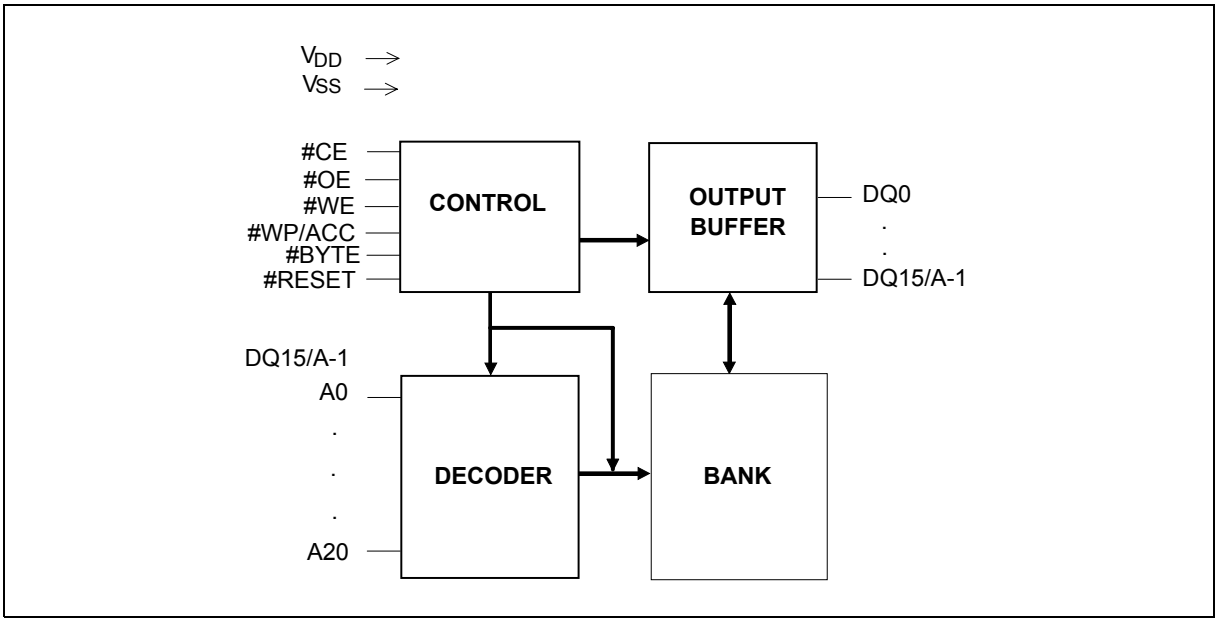
3. PIN CONFIGURATIONS

48-Ball TFBGA
(Top View, Balls Face Down)

	1	2	3	4	5	6	7	8
A	A6 A13	B6 A12	C6 A14	D6 A15	E6 A16	F6 #BYTE	G6 DQ15/A-1	H6 Vss
B	A5 A9	B5 A8	C5 A10	D5 A11	E5 DQ7	F5 DQ14	G5 DQ13	H5 DQ6
C	A4 #WE	B4 #RESET	C4 NC	D4 A19	E4 DQ5	F4 DQ12	G4 V_{DD}	H4 DQ4
D	A3 RY/#BY	B3 #WP/ACC	C3 A18	D3 A20	E3 DQ2	F3 DQ10	G3 DQ11	H3 DQ3
E	A2 A7	B2 A17	C2 A6	D2 A5	E2 DQ0	F2 DQ8	G2 DQ9	H2 DQ1
F	A1 A3	B1 A4	C1 A2	D1 A1	E1 A0	F1 #CE	G1 #OE	H1 Vss



4. BLOCK DIAGRAM



5. PIN DESCRIPTION

SYMBOL	PIN NAME	
A0–A20	Address Inputs	
DQ0–DQ14	Data Inputs/Outputs	
DQ15/A-1	Word mode	DQ15 is Data Inputs/Outputs
	Byte mode	A-1 is Address input
#CE	Chip Enable	
#OE	Output Enable	
#WE	Write Enable	
#WP/ACC	Hardware Write Protect/ Acceleration Pin	
#BYTE	Byte Enable Input	
#RESET	Hardware Reset	
RY/#BY	Ready/Busy Status	
V_{DD}	Power Supply	
V_{SS}	Ground	
NC	No Connection	

6. FUNCTIONAL DESCRIPTION

6.1 Device Bus Operation

6.1.1 Word/Byte Configuration

The #BYTE pin controls the device data I/O pins operate whether in the byte or word configuration. When the #BYTE pin is '1', the device is in word configuration; DQ0 -DQ15 are active and controlled by #CE and #OE.

When the #BYTE pin is '0', the device is in byte configuration, and only data I/O pins DQ0-DQ7 are active and controlled by #CE and #OE. The data I/O pins DQ8-DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

6.1.2 Reading Array Data

To read array data from the outputs, the #CE and #OE pins must be set to V_{IL}. #CE is the power control and used to select the device. #OE is the output control and gates array data to the output pins. #WE should stay at V_{IH}. The #BYTE pin determines the device outputs array data whether in words or bytes.

The internal state machine is set for reading array data when device power-up, or after hardware reset. This ensures that no excess modification of the memory content occurs during the power transition. In this mode there is no command necessary to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are changed.

6.1.3 Writing Commands/Command Sequences

In writhing a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive #WE and #CE to V_{IL}, and #OE to V_{IH}.

For program operations, the #BYTE pin determines the device accepts program data whether in bytes or in words. Refer to "Word/Byte Configuration" for more information.

The Unlock Bypass mode of device is to facilitate a faster programming. When a bank enters the Unlock Bypass mode, only two write cycles are required to program a word or byte. Please refer to "Word/Byte Configuration" section for details on programming data to the device using both standard and Unlock Bypass command sequences.

The erase operation can erase a sector, multiple sectors, even the entire device. The "sector address" is the address bits required to solely select a sector.

Accelerated Program Operation

The device provides accelerated program operations through the ACC function. This is one of two functions provided by the #WP/ACC pin. This function is primarily intended to allow a faster manufacturing throughput in the factory.

If #WP/ACC pin is set at V_{HH}, the device automatically enters into the Unlock Bypass mode. Then the device will temporarily unprotect any protected sectors, and uses the higher voltage on this pin to reduce the time required for program operations. The system would use a two-cycle program command sequence required by the Unlock Bypass mode. When V_{HH} is removed from the #WP/ACC pin, the device is back to a normal operation.

Please note that the #WP/ACC pin can not be at V_{HH} for operations except accelerated programming; otherwise, the device will be damaged. In addition, the #WP/ACC pin can not be left floating; otherwise, an unconnected inconsistent behavior will occur.

AUTOSELECT Functions

When the system writes the AUTOSELECT command sequence, the device enters the AUTOSELECT mode. The system can then read AUTOSELECT codes from the internal register (which is separate from the memory array) on DQ0 –DQ7. The standard read cycle timings are applied in this mode. Please refer to the AUTOSELECT Mode and AUTOSELECT Command Sequence sections for more information.

6.1.4 Standby Mode

When the system is not reading or writing to the device, the device will be in a standby mode. In this mode, current consumption is greatly reduced, and the outputs are in the high impedance state, independent from the #OE input.

When the #CE and #RESET pins are both held at $V_{DD} \pm 0.3V$, the device enters into the CMOS standby mode (note that this is a more restricted voltage range than V_{IH}.) When #CE and #RESET are held at V_{IH}, but not within $V_{DD} \pm 0.3V$, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

When the device is deselected during erasing or programming, the device initiates active current until the operation is completed.

6.1.5 Automatic Sleep Mode

The automatic sleep mode minimizes device's energy consumption. When addresses remain stable for t_{ACC} + 30ns, the device will enable this mode automatically. The automatic sleep mode is independent from the #CE, #WE, and #OE control signals. Standard address access timings provide new data when addresses are changed. In sleep mode, output data is latched and always available to the system.

6.1.6 #RESET: Hardware Reset Pin

The #RESET pin provides a hardware method to reset the device to reading array data. When the #RESET pin is set to low for at least a period of t_{RP}, the device will immediately terminate every operation in progress, tri-states all output pins, and ignores all read/write commands for the duration of the #RESET pulse. The device also resets the internal state machine to reading array data mode. To ensure data integrity, the interrupted operation needs to be reinitiated when the device is ready to accept another command sequence.

Current is reduced for the duration of the #RESET pulse. When #RESET is held at $V_{SS} \pm 0.3V$, the device initiates the CMOS standby current (I_{CC4}). If #RESET is held at V_{IL} but not within $V_{SS} \pm 0.3V$, the standby current will be greater.

The #RESET pin may be tied to the system-reset circuitry. Thus the system reset would also reset the device, enabling the system to read the boot-up firmware from the device.

If #RESET is asserted during the program or erase operation, the RY/#BY pin will be at “0” (busy) until the internal reset operation is complete. If #RESET is asserted when a program or erase operation is not processing (RY/#BY pin is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). After the #RESET pin returns to V_{IH}, the system can read data t_{RH}.

6.1.7 Output Disable Mode

When the #OE input is at V_{IH}, output from the device is disabled. The output pins are set in the high impedance state.

6.1.8 autoselect Mode

The AUTOSELECT mode offers manufacturer and device identification, as well as sector protection verification, through identifier codes output on DQ0-DQ7. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the AUTOSELECT codes can also be accessed in-system through the command register.

When using programming equipment, the AUTOSELECT mode requires V_{ID} (8.5V to 11.5V) on address pins A9. Address pins A6, A1, and A0 must be as shown in table. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ0-DQ7.

6.1.9 Sector/Sector Block Protection and Unprotection

The hardware sector protection feature disables both program and erasure operations in any sectors. The hardware sector Unprotection feature re-enables both program and erasure operations in previously protected sectors. Sector Protection/Unprotection can be implemented through two methods.

The primary method requires V_{ID} on the #RESET pin, and can be implemented either in-system or through programming equipment. This method uses standard microprocessor bus cycle timing.

The alternate method intended only for programming equipment requires V_{ID} on address pin A9 and #OE. It is possible to determine whether a sector is protected or unprotected. See the Application Note for detail information.

6.1.10 Write Protect (#WP)

The Write Protect function provides a hardware method to protect the certain boot sectors without using V_{ID}. This function is one of two features provided by the #WP/ACC pin.

When the #WP/ACC pin is set at V_{IL}, the device disables program and erase functions in the two outermost 8 Kbytes boot sectors independently of whether those sectors were protected or unprotected using the method described in “Sector/Sector Block Protection and Unprotection.” The two outermost 8 Kbytes boot sectors are the two sectors containing either the lowest addresses in a bottom-boot-configured device or the highest addresses in a top-boot-configured device.

When the #WP/ACC pin is set at V_{IH}, the device reverts to the two outermost 8 Kbytes boot sectors were last set either to be protected or unprotected. That is, sector Protection or Unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in “Sector/Sector Block Protection and Unprotection”.

Please note that the #WP/ACC pin must not be left floating or unconnected; otherwise, the inconsistent behavior of the device may occur.

6.1.11 Temporary Sector Unprotect

This feature allows temporary Unprotection of previously protected sectors to change data in-system. When the #RESET pin is set to V_{ID}, the Sector Unprotect mode is activated. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. What if V_{ID} is removed from the #RESET pin, all the previously protected sectors are protected again.

6.1.12 Security Sector Flash Memory Region

The Security Sector feature provides an OTP memory region that enables permanent device identification through an Electronic Serial Number (ESN). The Security Sector uses a Security Sector Indicator Bit (DQ7) to indicate whether the Security Sector is locked or not when shipped from the factory. The DQ7 is permanently set when it is in the factory and cannot be changed, which prevents copying of a factory locked part. This ensures the security of the ESN when the product is shipped to the field. This issue should be considered during system design. Winbond offers the device with the Security Sector either factory locked or customer lockable. The factory-locked version is always protected when shipped from the factory, and has the Security Sector Indicator Bit permanently set to "1" The customer-lockable version is shipped with the Security Sector unprotected, which allowing customers to utilize the sector in any ways they choose. The customer-lockable version has the Security Sector Indicator Bit permanently set to "0." Thus, the Security Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked.

The system accesses the Security Sector through a command sequence (see "Enter Security Sector/Exit Security Sector Command Sequence"). After the system has written the Enter Security Sector command sequence, it may read the Security Sector by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit Security Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the boot sectors.

Factory Locked: Security Sector Programmed and Protected At the Factory

The device Security Sector is protected when it is shipped from the factory, and it cannot be modified in any way. The device is available to be preprogrammed by one of the following:

- A random, secure ESN only
- Customer code through the supplier's service
- Both a random, secure ESN and customer code through supplier's service.

In devices with an ESN, the Bottom Boot device will be with the 16-byte ESN in the lowest addressable memory area at addresses 000000h–000007h in word mode (or 000000h–00000Fh in byte mode). In the Top Boot device the starting address of the ESN will be at the bottom of the highest 8 Kbytes boot sector at addresses 1FF000h–1FF007h in word mode (or addresses 3FE000h–3FE00Fh in byte mode). Customers may choose have their code programmed by Winbond. Winbond can program the customer's code, with or without the random ESN. The devices are then shipped with the Security Sector permanently locked.

Customer Lockable: Security Sector NOT Programmed or Protected At the Factory

If the security feature is not necessary, the Security Sector can be seen as an additional OTP memory space. When in system design, this issue should be considered. The Security Sector can be read, programmed; but cannot be erased. Please note that when programming the Security Sector, the accelerated programming (ACC) and unlock bypass functions are not available. The Security Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter Security Sector Region command sequence, and then follow the in-system sector protect algorithm, except that #RESET may be at either V_{IH} or V_{ID}. This allows in-system protection of the Security Sector without raising any device pin to a high voltage.
  Please note that this method is only suitable for the Security Sector.
- To verify the protect/unprotect status of the Security Sector; follow the algorithm show in Security Sector Protect Verify.

The Security Sector protection must be used with caution, since there is no procedure available for unprotect the Security Sector area and none of the bits in the Security Sector memory space can be modified in any ways.

6.1.13 Hardware Data Protection

The command sequence requirements of unlock cycles for programming or erasing provides data protection against negligent writes. In addition, the following hardware data protection measures prevent inadvertent erasure or programming, which might be caused by spurious system level signals during V_{DD} power-up and power-down transitions, or from system noise.

Write Pulse "Glitch" Protection

Noise pulses, which is less than 5 ns (typical) on #OE, #CE or #WE, do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of #OE = V_{IL}, #CE = V_{IH} or #WE = V_{IH}. #CE and #WE must be a logical zero while #OE is a logical one to initiate a write cycle.

Power-Up Write Inhibit

During power up, if #WE = #CE = V_{IL} and #OE = V_{IH}, the device does not accept commands on the rising edge of #WE. The internal state machine is automatically reset to the read mode on power-up.

6.2 Command Definitions

The device operation can be initiated by writing specific address and data commands or sequences into the command register. The device will be reset to reading array data when writing incorrect address and data values or writing them in the improper sequence.

The addresses will be latched on the falling edge of #WE or #CE, whichever happens later; while the data will be latched on the rising edge of #WE or #CE, whichever happens first. Please refer to timing waveforms.

6.2.1 Reading Array Data

After device power-up, it is automatically set to reading array data. There is no commands are required to retrieve data. After completing an Embedded Program or Embedded Erase algorithm, each bank is ready to read array data.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode. After it the system can read data from any non-erase-suspended sector within the same bank. And then, after completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. Please refer to Erase Suspend/Erase Resume Commands section for detail information.

The system must initiate the reset command to return a bank to read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or the bank is in the AUTOSELECT mode. See Reset Command section and Requirements for Reading Array Data in the Device Bus Operations section for more information.

6.2.2 Reset Command

The banks will be to the read or erase-suspend-read mode when writing the reset command. For this command, the address bits are Don't Care.

The reset command may be written between the sequential cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank, to which the system was writing to the read mode. If the program command sequence is written to a bank, in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. When programming begins, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an AUTOSELECT command sequence. When in the AUTOSELECT mode, the reset command must be written to return to the read mode. If a bank entered into the AUTOSELECT mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

6.2.3 AUTOSELECT Command Sequence

The AUTOSELECT command sequence provides the host system to access the manufacturer and device codes, and determine whether a sector is protected or not. This is an alternative method, which is intended for PROM programmers and requires V_{ID} on address pin A9. The AUTOSELECT command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. When the device is actively programming or erasing in the other bank, the AUTOSELECT command may not be written.

The first writing two unlock cycles initiate the AUTOSELECT command sequence. This is followed by a third write cycle that contains the bank address and the AUTOSELECT command. The bank then enters into the AUTOSELECT mode. The system may read at any address within the same bank without initiating another AUTOSELECT command sequence:

- A read cycle at address (BA) XX00h (where BA is the bank address) returns the manufacturer code.
- A read cycle at address (BA) XX01h in word mode (or (BA) XX02h in byte mode) returns the device code.
- A read cycle to an address containing a sector address (SA) within the same bank, and the address 02h on A7-A0 in word mode (or the address 04h on A6-A-1 in byte mode) returns 01h if the sector is protected or 00h if it is unprotected.

To return to read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend), the system must write the reset command.

Enter Security Sector/Exit Security Sector Command Sequence

The Security Sector region provides a secured data area containing a random, sixteen-byte electronic serial number (ESN). The system can access the Security Sector region by issuing the three-cycle

Enter Security Sector command sequence. The device continues to access the Security Sector region until the system issues the four-cycle Exit Security Sector command sequence. The Exit Security Sector command sequence returns the device to normal operation. See “Security Sector Flash Memory Region” for further information.

6.2.4 Byte/Word Program Command Sequence

The device can be programmed either by word or byte, which depending on the state of the #BYTE pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program setup command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The device automatically provides internally generated program pulses and verifies the programmed cell margin.

Once the Embedded Program algorithm is complete, the bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/#BY. Please refer to the Write Operation Status section for bits' information.

Any commands written to the device during the Embedded Program Algorithm are ignored. Please note that a hardware reset will immediately stop the program operation. The program command sequence should be reinitiated when the bank has returned to the read mode, in order to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from “0” back to “1.” If trying to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate that the operation is successful. However, a succeeding read will show that the data is still “0.” Only erase operations can change “0” to “1.”

6.2.5 Unlock Bypass Command Sequence

The unlock bypass feature provides the system to program bytes or words to a bank which is faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. And a third write cycle containing the unlock bypass command, 20h, is followed. Then, the bank enters into the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. In the same manner, additional data is programmed. This mode dispenses with the initial two unlock cycles which required in the standard program command sequence, resulting in faster total programming time.

All through the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. The system must issue the two-cycle unlock bypass reset command sequence to exit the unlock bypass mode. The first cycle must contain the bank address and the data 90h. The second cycle needs to contain the data 00h. Then, the bank returns to the read mode.

The device offers accelerated program operations by the #WP/ACC pin. When the V_{HH} is set at the #WP/ACC pin, the device automatically enters into the Unlock Bypass mode. Then, the two-cycle Unlock Bypass program command sequence may be written. To accelerate the operation, the device must use the higher voltage on the #WP/ACC pin. Please note that the #WP/ACC pin must not be at V_{HH} in any operation other than accelerated programming; otherwise the device may be damaged. In addition, the #WP/ACC pin must not be left floating or unconnected; otherwise the device inconsistent behavior may occur.

6.2.6 Chip Erase Command Sequence

Chip erase is a six-bus cycle operation. Writing two unlock cycles initiate the chip erase command sequence, which is followed by a set-up command. After chip erase command, two additional unlock write cycles are then followed, which in turn invokes the Embedded Erase algorithm. The system preprogram is not required prior to erase. Before electrical erase, the Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern. Any controls or timings during these operations is not required in system.

As the Embedded Erase algorithm is complete, the bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/#BY. Please refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation will be ignored. However, a hardware reset shall terminate the erase operation immediately. If this happens, to ensure data integrity, the chip erase command sequence should be reinitiated when that bank has returned to reading array data.

6.2.7 Sector Erase Command Sequence

Sector erase is a six-bus cycle operation. Writing two unlock cycles initiate the sector erase command sequence, which is followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command.

The device does not require the system to preprogram before erase. Before electrical erase, the Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern. Any controls or timings during these operations are not required in system.

A sector erase time-out of 50 μs occurs after the command sequence is written. Additional sector addresses and sector erase commands may be written during the time-out period. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 μs; otherwise, erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. To ensure all commands are accepted, processor interrupts be disabled during this time is recommended. The interrupts can be re-enabled after the last Sector Erase command is written. Any command other than Sector Erase or Erase Suspend during the time-out period resets the bank to the read mode. The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine whether or not the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final #WE pulse in the command sequence.

As the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Please note that when the Embedded Erase operation is in progress, the system can read data from the non-erasing bank at the same time. By reading DQ7, DQ6, DQ2, or RY/#BY in the erasing bank, the system can determine the status of the erase operation. Please refer to the Write Operation Status section for information on these status bits.

When the sector erase operation begins, only the Erase Suspend command is valid. All other commands are ignored. However, a hardware reset shall terminate the erase operation immediately. If

this occurs, to ensure data integrity, the sector erase command sequence should be reinitiated once the bank has returned to reading array data.

6.2.8 Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. When writing this command, the bank address is required. This command is valid only during the sector erase operation, which includes the 50 μs time-out period during the sector erase command sequence. If written during the chip erase operation or Embedded Program algorithm, the Erase Suspend command is ignored.

As the Erase Suspend command is written during the sector erase operation, a maximum of 20 μs is required to suspend the erase operation. However, while the Erase Suspend command is written during the sector erase time-out, the device shall terminate the time-out period and suspends the erase operation immediately.

The bank enters into an erase-suspend-read mode after the erase operation has been suspended. The system can read data from, or program data to, any sector not selected for erasure. (In device "erase suspends" all sectors are selected for erasure.) The "reading at any address within erase-suspended sectors produces status" information is on DQ0-DQ7. The system can use DQ7, or DQ6 and DQ2 together, to determine whether a sector is actively erasing or is erase-suspended. Please refer to the Write Operation Status section for detail information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. Using the DQ7 or DQ6 status bits, the system can determine the status of the program operation, just as in the standard Byte Program operation. Please refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the AUTOSELECT command sequence also can be issued. Please refer to the AUTOSELECT Mode and AUTOSELECT Command Sequence sections for details.

The Erase Resume command must be written to resume the sector erase operation. When writing this command, the bank address of the erase-suspended bank is required. Further writes of the Resume command are ignored. After the chip has resumed erasing, another Erase Suspend command can be written.

6.3 Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Each of DQ7 and DQ6 provides a method for determining whether a program or erase operation is complete or in progress. The device also offers a hardware-based output signal, RY/#BY, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

6.3.1 DQ7: #Data Polling

The #Data Polling bit, DQ7, indicates whether an Embedded Program or Erase algorithm is in progress or completed, or whether or not a bank is in Erase Suspend. Data Polling is valid after the rising edge of the final #WE pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 and the complement of the data programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. Once the Embedded Program algorithm has completed that the device outputs the data programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program

address falls within a protected sector, #Data Polling on DQ7 is active for about 1μs, and then that bank returns to the read mode.

During the Embedded Erase algorithm, #Data Polling produces "0" on DQ7. Once the Embedded Erase algorithm has completed, or when the bank enters the Erase Suspend mode, #Data Polling produces "1" on DQ7. An address within any of the sectors selected for erasure must be provided to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, #Data Polling on DQ7 is active for about 100 μs, and then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just before the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0-DQ6 while Output Enable (#OE) is set to low. That is, the device may change from providing status information to valid data on DQ7. Depending on when it samples the DQ7 output, the system may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0-DQ6 may be still invalid. Valid data on DQ0-DQ7 will appear on successive read cycles.

6.3.2 RY/#BY: Ready/#Busy

The RY/#BY is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/#BY status is valid after the rising edge of the final #WE pulse in the command sequence. Since RY/#BY is an open-drain output, several RY/#BY pins can be tied together in parallel with a pull-up resistor to V_{DD}.

When the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) When the output is high (Ready), the device is in the read mode, the standby mode, or one of the banks is in the erase-suspend-read mode.

6.3.3 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final #WE pulse in the command sequence (before the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either #OE or #CE to control the read cycles. Once the operation has completed, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for about 100 μs, and then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors which are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. If the device is actively erasing (i.e., the Embedded Erase algorithm is in progress), DQ6 toggles. While if the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see DQ7: #Data Polling).

If a program address falls within a protected sector, DQ6 toggles for about 1 μs after the program command sequence is written, and then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling when the Embedded Program algorithm is complete.

Please also refer to DQ2: Toggle Bit II.

6.3.4 DQ2: Toggle Bit II

When used with DQ6, the "Toggle Bit II" on DQ2 indicates whether a particular sector is actively erasing (i.e., the Embedded Erase algorithm is in progress), or the sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final #WE pulse in the command sequence.

DQ2 toggles as the system reads at addresses within those sectors that have been selected for erasure. (The system may use either #OE or #CE to control the read cycles.) But DQ2 cannot distinguish that whether the sector is actively erasing or is erase-suspended. By comparison, DQ6 indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Therefore, both status bits are required for sector and mode information.

6.3.5 Reading Toggle Bits DQ6/DQ2

Whenever the system initially starts to read toggle bit status, it must read DQ0-DQ7 at least twice in a row to determine whether a toggle bit is toggling or not. Typically, the system would note and store the value of the toggle bit after the first read. While after the second read, the system would compare the new value of the toggle bit with the first one. If the toggle bit is not toggling, the device has completed the program or erasure operation. The system can read array data on DQ0-DQ7 on the following read cycle.

However, if after the initial two read cycles, the system finds that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high or not(see the section on DQ5). If DQ5 is high, the system should then determine again whether the toggle bit is toggling or not, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erasure operation. If it is still toggling, the device did not complete the operation, and the system must write the reset command to return to reading array data.

Then the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, and determines the status as described in the previous paragraph. Alternatively, the system may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm while it returns to determine the status of the operation.

6.3.6 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. DQ5 produces "1" under these conditions which indicates that the program or erase cycle was not successfully completed.

The device may output "1" on DQ5 if the system tries to program "1" to a location that was previously programmed to "0." Only the erase operation can change "0" back to "1." Under this condition, the device stops the operation, and while the timing limit has been exceeded, DQ5 produces "1."

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

6.3.7 DQ3: Sector Erase Timer

After writing a sector erasure command sequence, the system may read DQ3 to determine whether erasure has begun or not. (The sector erase timer does not apply to the chip erase command.) The entire time-out applies after each additional sector erasure command if additional sectors are selected for erasure. Once the timeout period has completed, DQ3 switches from “0” to “1.” If the time between additional sector erase commands from the system can be assumed to be less than 50 μs, the system need not monitor, DQ3 does not need to be monitored. Please also refer to Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (#Data Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is“1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device will accept additional sector erase commands.

The system software should check the status of DQ3 before and following each subsequent sector erase command to ensure the command has been accepted. If DQ3 is high on the second status check, the last command might not have been accepted.

7. TABLE OF OPERATION MODES

7.1 Device Bus Operations

MODE	#CE	#OE	#WE	#RESET	#WP/ACC	ADDRESSES	DQ0-DQ7	DQ8-DQ15	
								#BYTE=VIH	#BYTE =VIL
Read	L	L	H	H	L/H	AIN	DOUT	DOUT	DQ8-DQ14
Write	L	H	L	H	(Note2)	AIN	DIN	DIN	=High-Z, DQ15=A-1
Standby	VDD ±0.3V	X	X	VDD ±0.3V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z
Sector Protect	L	H	L	VID	L/H	SA, A6=L, A1=H, A0=L	DIN	X	X
Sector Unprotect	L	H	L	VID	(Note2)	SA, A6=H, A1=H, A0=L	DIN	X	X
Temporary Sector Unprotect	X	X	X	VID	(Note2)	AIN	DIN	DIN	High-Z

Legend: L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 8.5 ~ 11.5 V, V_{HH} = 9.0 ± 0.5 V, X = Don't Care, SA = Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out.

Notes:

1. Addresses are A20:A0 in word mode (#BYTE = V_{IH}), A20: A-1 in byte mode (#BYTE = V_{IL}).
2. If #WP/ACC = V_{IL}, the two outermost boot sectors remain protected. If #WP/ACC = V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotect ion". If #WP/ACC = V_{HH}, all sectors will be unprotected.

7.2 AUTOSELECT Codes (High Voltage Method)

DESCRIPTION	#CE	#OE	#WE	A20 TO A12	A11 TO A10	A9	A8 TO A7	A6	A5 TO A2	A1	A0	DQ8 TO DQ15		DQ7 TO DQ0
												#BYTE = VIH	#BYTE = VIL	
Manufacturer ID: Winbond	VIL	VIL	VIH	X	X	VID	X	VIL	X	VIL	VIL	X	X	DAh
Device ID: W19B320BT (Top Boot Block)	VIL	VIL	VIH	X	X	VID	X	VIL	X	VIL	VIH	22h	X	BAh
Device ID: W19B320BB (Bottom Boot Block)	VIL	VIL	VIH	X	X	VID	X	VIL	X	VIL	VIH	22h	X	2Ah
Sector Protection Verification	VIL	VIL	VIH	SA	X	VID	X	VIL	X	VIH	VIL	X X	X X	01h (protected) 00h (unprotected)
Security Indicator Bit (DQ7)	VIL	VIL	VIH	X	X	VID	X	VIL	X	VIH	VIH	X	X	82h (factory locked) 02h (not factory locked)

Legend: SA= Sector Address, X= Don't Care.

7.3 Sector Address Table (Top Boot Block)

SECTOR	SECTOR ADDRESS A20-A12	SECTOR SIZE (KBYTES/KWORDS)	(X8) ADDRESS RANGE	(X16) ADDRESS RANGE
SA0	000000XXX	64/32	000000h-00FFFFh	000000h-07FFFh
SA1	000001XXX	64/32	010000h-01FFFFh	008000h-0FFFFh
SA2	000010XXX	64/32	020000h-02FFFFh	010000h-17FFFh
SA3	000011XXX	64/32	030000h-03FFFFh	018000h-01FFFFh
SA4	000100XXX	64/32	040000h-04FFFFh	020000h-027FFFh
SA5	000101XXX	64/32	050000h-05FFFFh	028000h-02FFFFh
SA6	000110XXX	64/32	060000h-06FFFFh	030000h-037FFFh
SA7	000111XXX	64/32	070000h-07FFFFh	038000h-03FFFFh
SA8	001000XXX	64/32	080000h-08FFFFh	040000h-047FFFh
SA9	001001XXX	64/32	090000h-09FFFFh	048000h-04FFFFh
SA10	001010XXX	64/32	0A0000h-0AFFFFh	050000h-057FFFh
SA11	001011XXX	64/32	0B0000h-0BFFFFh	058000h-05FFFFh
SA12	001100XXX	64/32	0C0000h-0CFFFFh	060000h-067FFFh
SA13	001101XXX	64/32	0D0000h-0DFFFFh	068000h-06FFFFh
SA14	001110XXX	64/32	0E0000h-0EFFFFh	070000h-077FFFh
SA15	001111XXX	64/32	0F0000h-0FFFFFh	078000h-07FFFFh
SA16	010000XXX	64/32	100000h-10FFFFh	080000h-087FFFh
SA17	010001XXX	64/32	110000h-11FFFFh	088000h-08FFFFh
SA18	010010XXX	64/32	120000h-12FFFFh	090000h-097FFFh
SA19	010011XXX	64/32	130000h-13FFFFh	098000h-09FFFFh
SA20	010100XXX	64/32	140000h-14FFFFh	0A0000h-0A7FFFh
SA21	010101XXX	64/32	150000h-15FFFFh	0A8000h-0AFFFFh
SA22	010110XXX	64/32	160000h-16FFFFh	0B0000h-0B7FFFh
SA23	010111XXX	64/32	170000h-17FFFFh	0B8000h-0BFFFFh
SA24	011000XXX	64/32	180000h-18FFFFh	0C0000h-0C7FFFh
SA25	011001XXX	64/32	190000h-19FFFFh	0C8000h-0CFFFFh
SA26	011010XXX	64/32	1A0000h-1AFFFFh	0D0000h-0D7FFFh
SA27	011011XXX	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
SA28	011100XXX	64/32	1C0000h-1CFFFFh	0E0000h-0E7FFFh
SA29	011101XXX	64/32	1D0000h-1DFFFFh	0E8000h-0EFFFFh
SA30	011110XXX	64/32	1E0000h-1EFFFFh	0F0000h-0F7FFFh
SA31	011111XXX	64/32	1F0000h-1FFFFFh	0F8000h-0FFFFFh
SA32	100000XXX	64/32	200000h-20FFFFh	100000h-107FFFh
SA33	100001XXX	64/32	210000h-21FFFFh	108000h-10FFFFh
SA34	100010XXX	64/32	220000h-22FFFFh	110000h-117FFFh

Sector Address Table (Top Boot Block), continued

SECTOR	SECTOR ADDRESS A20-A12	SECTOR SIZE (Kbytes/Kwords)	(X8) ADDRESS RANGE	(X16) ADDRESS RANGE
SA35	100011XXX	64/32	230000h-23FFFFh	118000h-11FFFFh
SA36	100100XXX	64/32	240000h-24FFFFh	120000h-127FFFh
SA37	100101XXX	64/32	250000h-25FFFFh	128000h-12FFFFh
SA38	100110XXX	64/32	260000h-26FFFFh	130000h-137FFFh
SA39	100111XXX	64/32	270000h-27FFFFh	138000h-13FFFFh
SA40	101000XXX	64/32	280000h-28FFFFh	140000h-147FFFh
SA42	101010XXX	64/32	2A0000h-2AFFFFh	150000h-157FFFh
SA43	101011XXX	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
SA44	101100XXX	64/32	2C0000h-2CFFFFh	160000h-167FFFh
SA45	101101XXX	64/32	2D0000h-2DFFFFh	168000h-16FFFFh
SA46	101110XXX	64/32	2E0000h-2EFFFFh	170000h-177FFFh
SA47	101111XXX	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
SA48	110000XXX	64/32	300000h-30FFFFh	180000h-187FFFh
SA49	110001XXX	64/32	310000h-31FFFFh	188000h-18FFFFh
SA50	110010XXX	64/32	320000h-32FFFFh	190000h-197FFFh
SA51	110011XXX	64/32	330000h-33FFFFh	198000h-19FFFFh
SA52	110100XXX	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
SA53	110101XXX	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
SA54	110110XXX	64/32	360000h-36FFFFh	1B0000h-1B7FFFh
SA55	110111XXX	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
SA56	111000XXX	64/32	380000h-38FFFFh	1C0000h-1C7FFFh
SA57	111001XXX	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
SA58	111010XXX	64/32	3A0000h-3AFFFFh	1D0000h-1D7FFFh
SA59	111011XXX	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
SA60	111100XXX	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
SA61	111101XXX	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
SA62	111110XXX	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
SA63	111111000	8/4	3F0000h-3F1FFFh	1F8000h-1F8FFFh
SA64	111111001	8/4	3F2000h-3F3FFFh	1F9000h-1F9FFFh
SA65	111111010	8/4	3F4000h-3F5FFFh	1FA000h-1FAFFFh
SA66	111111011	8/4	3F6000h-3F7FFFh	1FB000h-1FBFFFh
SA67	111111100	8/4	3F8000h-3F9FFFh	1FC000h-1FCFFFh
SA68	111111101	8/4	3FA000h-3FBFFFh	1FD000h-1FDFFFh
SA69	111111110	8/4	3FC000h-3FDFFFh	1FE000h-1FEFFFh
SA70	111111111	8/4	3FE000h-3FFFFFh	1FF000h-1FFFFFh

Note: The address range is [A20: A-1] in byte mode (#BYTE =V_{IL}) or [A20:A0] in word mode (#BYTE = V_{IH}).

Security Sector Addresses for Top Boot Devices

DEVICE	Sector Address A20-A12	SECTOR SIZE (bytes/words)	(X 8) ADDRESS RANGE	(X 16) ADDRESS RANGE
W19B320BT/B	111111XXX	256/128	3FE000h-3FE0FFh	1FF000h-1FF07Fh

7.4 Sector Address Table (Bottom Boot Block)

SECTOR	SECTOR ADDRESS A20-A12	SECTOR SIZE (Kbytes/Kwords)	(X8) ADDRESS RANGE	(X16) ADDRESS RANGE
SA0	000000000	8/4	000000h-001FFFh	000000h-000FFFh
SA1	000000001	8/4	002000h-003FFFh	001000h-001FFFh
SA2	000000010	8/4	004000h-005FFFh	002000h-002FFFh
SA3	000000011	8/4	006000h-007FFFh	003000h-003FFFh
SA4	000000100	8/4	008000h-009FFFh	004000h-004FFFh
SA5	000000101	8/4	00A000h-00BFFFh	005000h-005FFFh
SA6	000000110	8/4	00C000h-00DFFFh	006000h-006FFFh
SA7	000000111	8/4	00E000h-00FFFFh	007000h-007FFFh
SA8	000001XXX	64/32	010000h-01FFFFh	008000h-00FFFFh
SA9	000010XXX	64/32	020000h-02FFFFh	010000h-017FFFh
SA10	000011XXX	64/32	030000h-03FFFFh	018000h-01FFFFh
SA11	000100XXX	64/32	040000h-04FFFFh	020000h-027FFFh
SA12	000101XXX	64/32	050000h-05FFFFh	028000h-02FFFFh
SA13	000110XXX	64/32	060000h-06FFFFh	030000h-037FFFh
SA14	000111XXX	64/32	070000h-07FFFFh	038000h-03FFFFh
SA15	001000XXX	64/32	080000h-08FFFFh	040000h-047FFFh
SA16	001001XXX	64/32	090000h-09FFFFh	048000h-04FFFFh
SA17	001010XXX	64/32	0A0000h-0AFFFFh	050000h-057FFFh
SA18	001011XXX	64/32	0B0000h-0BFFFFh	058000h-05FFFFh
SA19	001100XXX	64/32	0C0000h-0CFFFFh	060000h-067FFFh
SA20	001101XXX	64/32	0D0000h-0DFFFFh	068000h-06FFFFh
SA21	001110XXX	64/32	0E0000h-0EFFFFh	070000h-077FFFh
SA22	001111XXX	64/32	0F0000h-0FFFFFh	078000h-07FFFFh
SA23	010000XXX	64/32	100000h-10FFFFh	080000h-087FFFh
SA24	010001XXX	64/32	110000h-11FFFFh	088000h-08FFFFh
SA25	010010XXX	64/32	120000h-12FFFFh	090000h-097FFFh
SA26	010011XXX	64/32	130000h-13FFFFh	098000h-09FFFFh
SA27	010100XXX	64/32	140000h-14FFFFh	0A0000h-0A7FFFh
SA28	010101XXX	64/32	150000h-15FFFFh	0A8000h-0AFFFFh
SA29	010110XXX	64/32	160000h-16FFFFh	0B0000h-0B7FFFh
SA30	010111XXX	64/32	170000h-17FFFFh	0B8000h-0BFFFFh
SA31	011000XXX	64/32	180000h-18FFFFh	0C0000h-0C7FFFh

Sector Address Table (Bottom Boot Block), continued

SECTOR	SECTOR ADDRESS A20-A12	SECTOR SIZE (Kbytes/Kwords)	(X8) ADDRESS RANGE	(X16) ADDRESS RANGE
SA32	011001XXX	64/32	190000h-19FFFFh	0C8000h-0CFFFFh
SA33	011010XXX	64/32	1A0000h-1AFFFFh	0D0000h-0D7FFFh
SA34	011011XXX	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
SA35	011100XXX	64/32	1C0000h-1CFFFFh	0E0000h-0E7FFFh
SA36	011101XXX	64/32	1D0000h-1DFFFFh	0E8000h-0EFFFFh
SA37	011110XXX	64/32	1E0000h-1EFFFFh	0F0000h-0F7FFFh
SA38	011111XXX	64/32	1F0000h-1FFFFFh	0F8000h-0FFFFFh
SA39	100000XXX	64/32	200000h-20FFFFh	100000h-107FFFh
SA40	100001XXX	64/32	210000h-21FFFFh	108000h-10FFFFh
SA41	100010XXX	64/32	220000h-22FFFFh	110000h-117FFFh
SA42	100011XXX	64/32	230000h-23FFFFh	118000h-11FFFFh
SA43	100100XXX	64/32	240000h-24FFFFh	120000h-127FFFh
SA44	100101XXX	64/32	250000h-25FFFFh	128000h-12FFFFh
SA45	100110XXX	64/32	260000h-26FFFFh	130000h-137FFFh
SA46	100111XXX	64/32	270000h-27FFFFh	138000h-13FFFFh
SA47	101000XXX	64/32	280000h-28FFFFh	140000h-147FFFh
SA48	101001XXX	64/32	290000h-29FFFFh	148000h-14FFFFh
SA49	101010XXX	64/32	2A0000h-2AFFFFh	150000h-157FFFh
SA50	101011XXX	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
SA51	101100XXX	64/32	2C0000h-2CFFFFh	160000h-167FFFh
SA52	101101XXX	64/32	2D0000h-2DFFFFh	168000h-16FFFFh
SA53	101110XXX	64/32	2E0000h-2EFFFFh	170000h-177FFFh
SA54	101111XXX	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
SA55	111000XXX	64/32	300000h-30FFFFh	180000h-187FFFh
SA56	110001XXX	64/32	310000h-31FFFFh	188000h-18FFFFh
SA57	110010XXX	64/32	320000h-32FFFFh	190000h-197FFFh
SA58	110011XXX	64/32	330000h-33FFFFh	198000h-19FFFFh
SA59	110100XXX	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
SA60	110101XXX	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
SA61	110110XXX	64/32	360000h-36FFFFh	1B0000h-1B7FFFh
SA62	110111XXX	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
SA63	111000XXX	64/32	380000h-38FFFFh	1C0000h-1C7FFFh
SA64	111001XXX	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
SA65	111010XXX	64/32	3A0000h-3AFFFFh	1D0000h-1D7FFFh
SA65	111011XXX	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
SA67	111100XXX	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
SA68	111101XXX	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
SA69	111110XXX	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
SA70	111111XXX	64/32	3F0000h-3FFFFFh	1F8000h-1FFFFFh

Note: The address range is [A20: A-1] in byte mode (#BYTE =V_{IL}) or [A20:A0] in word mode (#BYTE =V_{IH}).

Security Sector Addresses for Bottom Boot Devices

DEVICE	SECTOR ADDRESS A20-A12	SECTOR SIZE (BYTES/WORDS)	(X8) ADDRESS RANGE	(X16) ADDRESS RANGE
W19B320BT/B	000000XXX	256/128	000000h-0000FFh	000000h-00007Fh

7.5 Top Boot Sector/Sector Block Address for Protection/Unprotection)

SECTOR	A20-A12	SECTOR/SECTOR BLOCK SIZE
SA0-SA3	000000XXX 000001XXX 000010XXX 000011XXX	256(4x64) K bytes
SA4-SA7	0001XXXXX	256(4x64) K bytes
SA8-SA11	0010XXXXX	256(4x64) K bytes
SA12-SA15	0011XXXXX	256(4x64) K bytes
SA16-SA19	0100XXXXX	256(4x64) K bytes
SA20-SA23	0101XXXXX	256(4x64) K bytes
SA24-SA27	0110XXXXX	256(4x64) K bytes
SA28-SA31	0111XXXXX	256(4x64) K bytes
SA32-SA35	1000XXXXX	256(4x64) K bytes
SA36-SA39	1001XXXXX	256(4x64) K bytes
SA40-SA43	1010XXXXX	256(4x64) K bytes
SA44-SA47	1011XXXXX	256(4x64) K bytes
SA48-SA51	1100XXXXX	256(4x64) K bytes
SA52-SA55	1101XXXXX	256(4x64) K bytes
SA56-SA59	1110XXXXX	256(4x64) K bytes
SA60-SA62	111100XXX 111101XXX 111110XXX	192(3x64) K bytes
SA63	111111000	8 K bytes
SA64	111111001	8 K bytes
SA65	111111010	8 K bytes
SA66	111111011	8 K bytes
SA67	111111100	8 K bytes
SA68	111111101	8 K bytes
SA69	111111110	8 K bytes
SA70	111111111	8 K bytes

Bottom Boot Sector/Sector Block Address for Protection/Unprotection)

SECTOR	A20-A12	SECTOR/SECTOR BLOCK SIZE
SA70-SA67	111111XXX 111110XXX 111101XXX 111100XXX	256(4x64) K bytes
SA66-SA63	1110XXXXX	256(4x64) K bytes
SA62-SA59	1101XXXXX	256(4x64) K bytes
SA58-SA55	1100XXXXX	256(4x64) K bytes
SA54-SA51	1011XXXXX	256(4x64) K bytes
SA50-SA47	1010XXXXX	256(4x64) K bytes
SA46-SA43	1001XXXXX	256(4x64) K bytes
SA42-SA39	1000XXXXX	256(4x64) K bytes
SA38-SA35	0111XXXXX	256(4x64) K bytes
SA34-SA31	0110XXXXX	256(4x64) K bytes
SA30-SA27	0101XXXXX	256(4x64) K bytes
SA26-SA23	0100XXXXX	256(4x64) K bytes
SA22-SA19	0011XXXXX	256(4x64) K bytes
SA18-SA15	0010XXXXX	256(4x64) K bytes
SA14-SA11	0001XXXXX	256(4x64) K bytes
SA10-SA8	000011XXX 000010XXX 000001XXX	192(3x64) K bytes
SA7	000000111	8 K bytes
SA6	000000110	8 K bytes
SA5	000000101	8 K bytes
SA4	000000100	8 K bytes
SA3	000000011	8 K bytes
SA2	000000010	8 K bytes
SA1	000000001	8 K bytes
SA0	000000000	8 K bytes

7.6 CFI Query Identification String

DESCRIPTION	ADDRESS (Word Mode)	DATA	ADDRESS (Byte Mode)
Query-unique ASCII string "QRY"	10h 11h 12h	0051h 0052h 0059h	20h 22h 24h
Primary OEM Command Set	13h 14h	0002h 0000h	26h 28h
Address for primary Extended Table	15h 16h	0040h 0000h	2Ah 2Ch
Alternate OEM Command Set (00h = none exists)	17h 18h	0000h 0000h	2Eh 30h
Address for Alternative OEM Extended table (00h = none exists)	19h 1Ah	0000h 0000h	32h 34h

7.6.1 System Interface String

DESCRIPTION	ADDRESS (Word Mode)	DATA	ADDRESS (Byte Mode)
VDD Min. (write/erase) D7-D4: volt , D3-D0: 100 mV	1Bh	0027h	36h
VDD Max. (write/erase) D7-D4: volt , D3-D0: 100 mV	1Ch	0036h	38h
VPP Min. voltage (00h=no V_{PP} pin present)	1Dh	0000h	3Ah
VPP Max. voltage (00h=no V_{PP} pin present)	1Eh	0000h	3Ch
Typical timeout per single byte/word write 2^N μs	1Fh	0004h	3Eh
Typical timeout for Min. size buffer write 2^N μs (00h=not supported)	20h	0000h	40h
Typical timeout per individual block erase 2^N ms	21h	000Ah	42h
Typical timeout for full chip erase 2^N ms (00h=not supported)	22h	0000h	44h
Max. timeout for byte/word write 2^N times typical	23h	0005h	46h
Max. timeout for buffer write 2^N times typical	24h	0000h	48h
Max. timeout per individual block erase 2^N times typical	25h	0004h	4Ah
Max. timeout for full chip erase 2^N times typical (00h = not supported)	26h	0000h	4Ch

7.6.2 Device Geometry Definition

DESCRIPTION	ADDRESS (Word Mode)	DATA	ADDRESS (Byte Mode)
Device size =2^N bytes	27h	0016h	4Eh
Flash device interface description (refer to CFI publication 100)	28h	0002h	50h
	29h	0000h	52h
Max. number of bytes in multi-byte write=2^N (00h=not supported)	2Ah	0000h	54h
	2Bh	0000h	56h
Number of Erase Block Regions within devices	2Ch	0002h	58h
Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)	2Dh	0007h	5Ah
	2Eh	0000h	5Ch
	2Fh	0020h	5Eh
	30h	0000h	60h
Erase Block Region 2 Information	31h	003Eh	62h
	32h	0000h	64h
	33h	0000h	66h
	34h	0001h	68h
Erase Block Region 3 Information	35h	0000h	6Ah
	36h	0000h	6Ch
	37h	0000h	6Eh
	38h	0000h	70h
Erase Block Region 4 Information	39h	0000h	72h
	3Ah	0000h	74h
	3Bh	0000h	76h
	3Ch	0000h	78h

7.6.3 Primary Vendor-Specific Extended Query

DESCRIPTION	ADDRESS (Word Mode)	DATA	ADDRESS (Byte Mode)
Query-unique ASCII string "PRI"	40h 41h 42h	0050h 0052h 0049h	80h 82h 84h
Major version number, ASCII	43h	0031h	86h
Minor version number, ASCII	44h	0033h	88h
Silicon Revision Number 01h = 0.13 μm	45h	0001h	8Ah
Erase suspend 0 = Not supported, 1= To read only; 2 = To read & write	46h	0002h	8Ch
Sector protect 00 = Not supported, 01=Supported	47h	0001h	8Eh
Sector Temporary Unprotect 00 = Not supported, 01=Supported	48h	0001h	90h
Sector protect/unprotect scheme	49h	0004h	92h
Simultaneous operation Number of Sectors (except for Bank 1)	4Ah	0038h	94h
Burst mode type 00 = Not supported, 01=Supported	4Bh	0000h	96h
Page mode type 00 = Not Supported, 01=4 Word Page, 02=8 Word Page	4Ch	0000h	98h
ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV	4Dh	0085h	9Ah
ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV	4Eh	0095h	9Ch
Top/Bottom Boot Sector Flag 02h=Bottom Boot Device, 03h=Top Boot Device	4Fh	000Xh	9Eh

7.6.4 Command Definitions

COMMAND SEQUENCE (note 1)		CYCLE	BUS CYCLES (note 2-5)											
			FIRST		SECOND		THIRD		FOURTH		FIFTH		SIXTH	
			ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA
Read (note 6)		1	RA	RD										
Reset (note 7)		1	XXX	F0										
Normal Program	Word	4	555	AA	2AA	55	555	A0	PA	PD				
	Byte		AAA		555		AAA							
Unlock Bypass	Word	3	555	AA	2AA	55	555	20						
	Byte		AAA		555		AAA							
Unlock Bypass Program (note 11)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (note12)		2	XXX	90	XXX	00								
Chip Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
	Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase	Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
	Byte		AAA		555		AAA		AAA		555			
Erase Suspend (note 13)		1	XXX	B0										
Erase Resume (note 14)		1	XXX	30										
AUTOSELECT(note8) Manufacturer Code	Word	4	555	AA	2AA	55	555	90	X00	DA				
	Byte		AAA		555		AAA							
AUTOSELECT(note8) Device Code	Word	4	555	AA	2AA	55	55	90	X01	(note 16)				
	Byte		AAA		555		AAA		X02					
AUTOSELECT(note8) Security Sector Factory Protect (Note 9)	Word	4	555	AA	2AA	55	555	90	X03	82/02				
	Byte		AAA		555		AAA		X06					
AUTOSELECT(note8) Sector/Sector Block Protect Verify (note 10)	Word	4	555	AA	2AA	55	555	90	X02	00/01				
	Byte		AAA		555		AAA		X04					
Enter Security Sector Region	Word	3	555	AA	2AA	55	555	88						
	Byte		AAA		555		AAA							
Exit Security Sector Region	Word	4	555	AA	2AA	55	555	90	XXX	00				
	Byte		AAA		555		AAA							
Common Flash Interface (CFI) Query (note 15)	Word	1	55	98										
	Byte		AA											

Legend:

X = Don't Care

RA = Address of the memory location to be read.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the #WE or #CE pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of #WE or #CE pulse, whichever happens first.

RD = Data read from location RA during read operation.

SA = Address of the sector to be verified (in AUTOSELECT mode) or erased. Address bits A20-A12 uniquely select any sector.

Notes:

1. See Bus Operations Table for details.
2. All values are in hexadecimal.
3. Except for the read cycle and the fourth cycle of the AUTOSELECT command sequence, all bus cycles are write cycles.
4. Data bits DQ15-DQ8 are don't care in command sequences, except for RD and PD.
5. Unless otherwise noted, address bits A20-A11 are "don't care".
6. No unlock or command cycles required when bank is reading array data.
7. The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when the device is in the AUTOSELECT mode, or if DQ5 goes high (while the device is providing status information).
8. The fourth cycle of the AUTOSELECT command sequence is a read cycle. Data bits DQ15-DQ8 are don't care. See the AUTOSELECT Command Sequence section for more information.
9. The data is 82h for factory locked and 02h for not factory locked.
10. The data is 00h for an unprotected sector/sector block and 01h for a protected sector/sector block.
11. The Unlock Bypass command is required prior to the Unlock Bypass Program command.
12. The Unlock Bypass Reset command is required to return to the read mode when the bank is in the unlock bypass mode.
13. The system may read and program in non-erasing sectors, or enter the AUTOSELECT mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
14. The Erase Resume command is valid only during the Erase Suspend mode.
15. Command is valid when device is ready to read array data or when device is in AUTOSELECT mode.
16. See Autoselect Codes table for device ID information

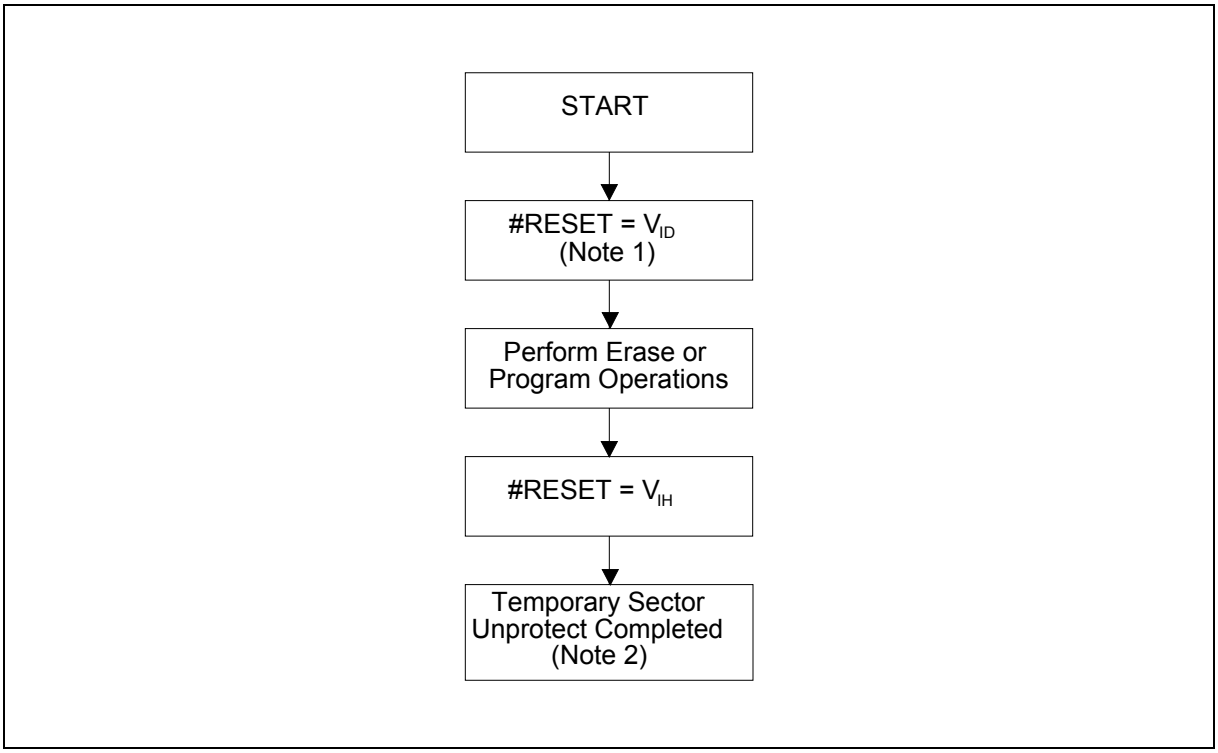
7.6.5 Write Operation Status

STATUS			DQ7 (NOTE 2)	DQ6	DQ5 (NOTE1)	DQ3	DQ2 (NOTE 2)	RY/#BY
Standard Mode	Embedded Program Algorithm		#DQ7	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		#DQ7	Toggle	0	N/A	N/A	0

Notes:

1. DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to DQ5 description section for more information.
2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
3. When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.

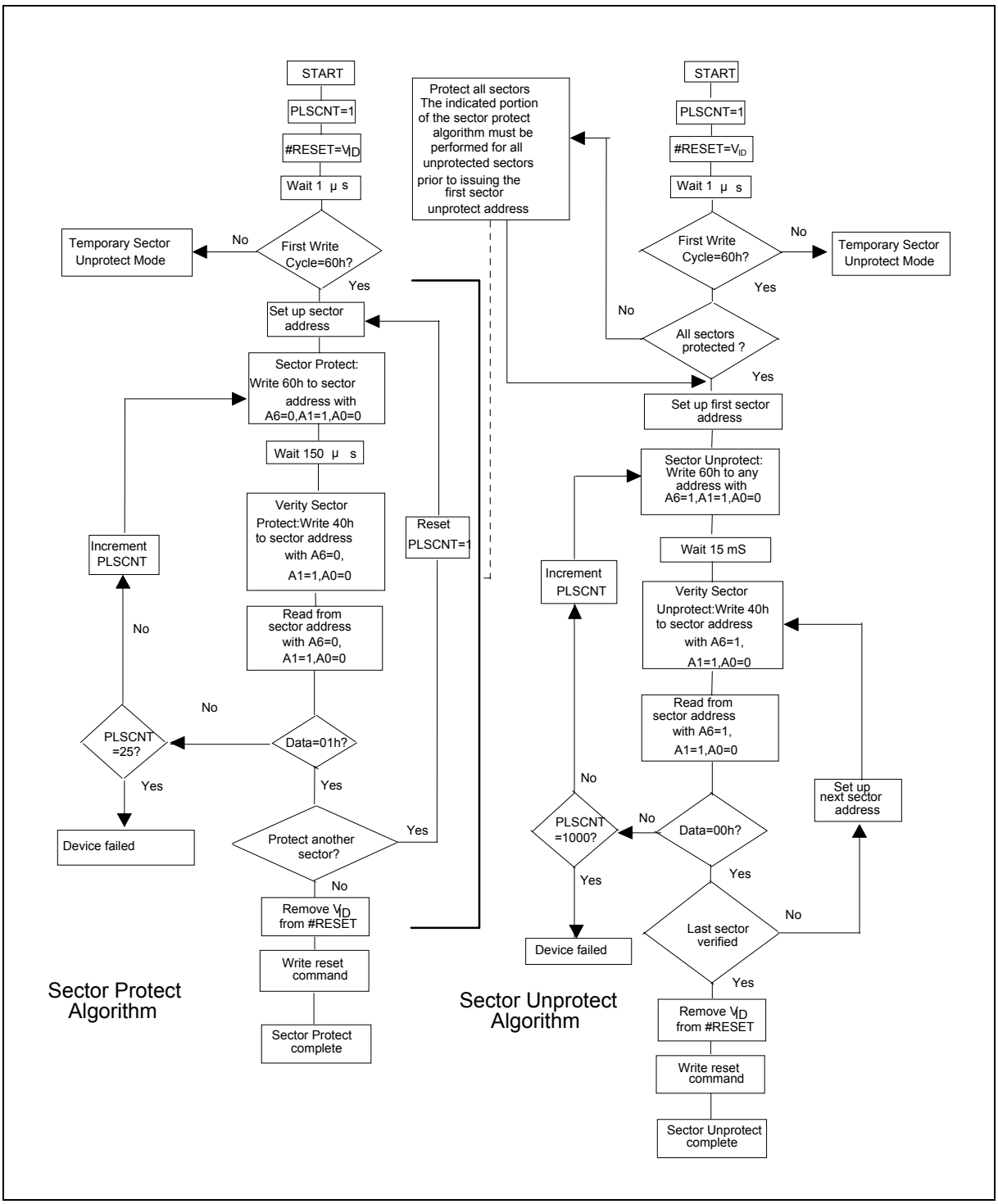
7.7 Temporary Sector Unprotect Algorithm



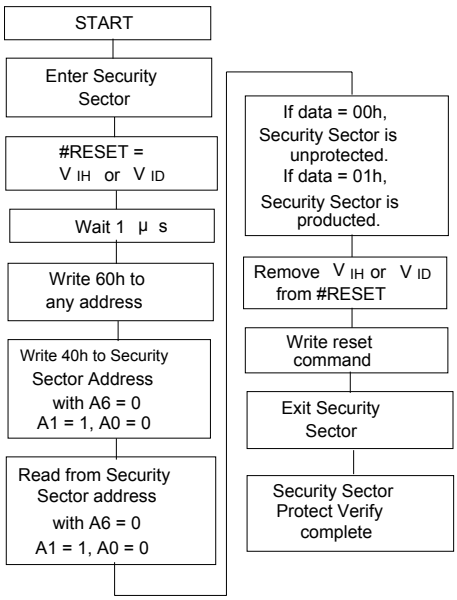
Notes:

1. All protected sectors unprotected (If #WP/ACC = VIL, outermost boot sectors will remain protected).
2. All previously protected sectors are protected once again.

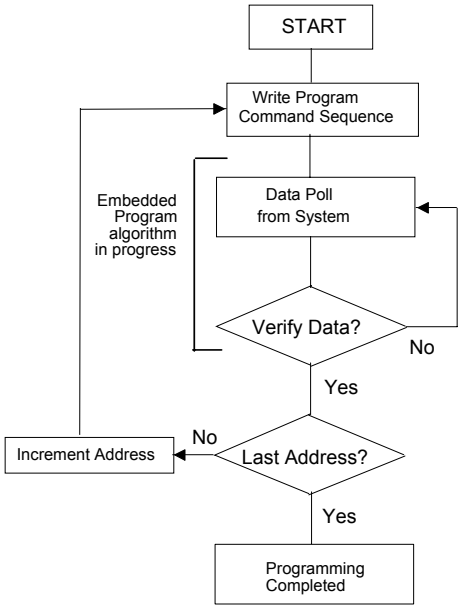
7.8 In-System Sector Protect/Unprotect Algorithms



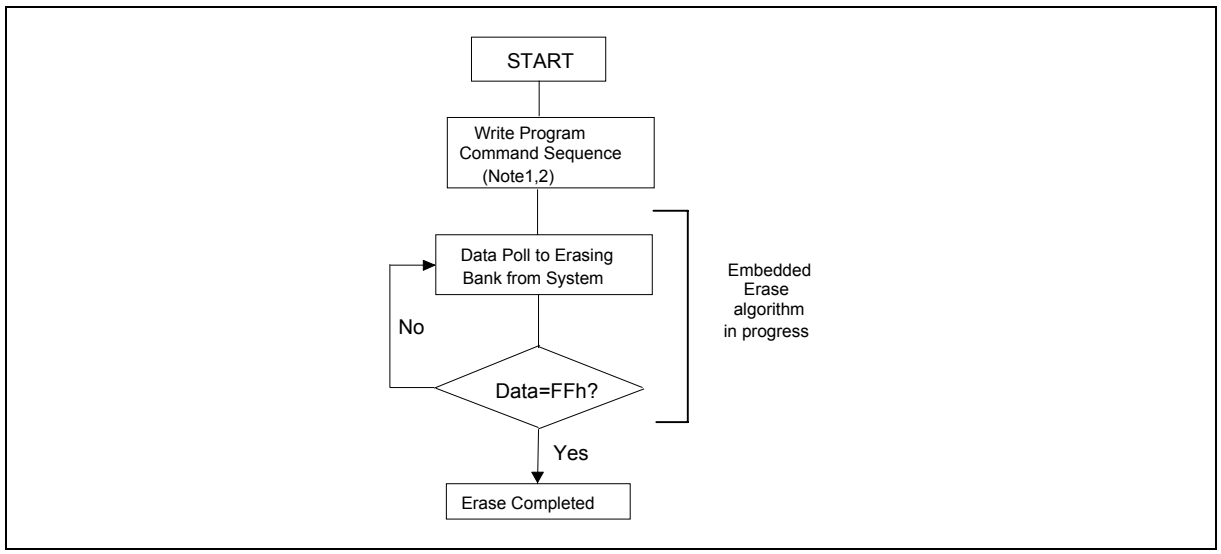
7.9 Security Sector Protect Verify



7.10 Program Algorithm



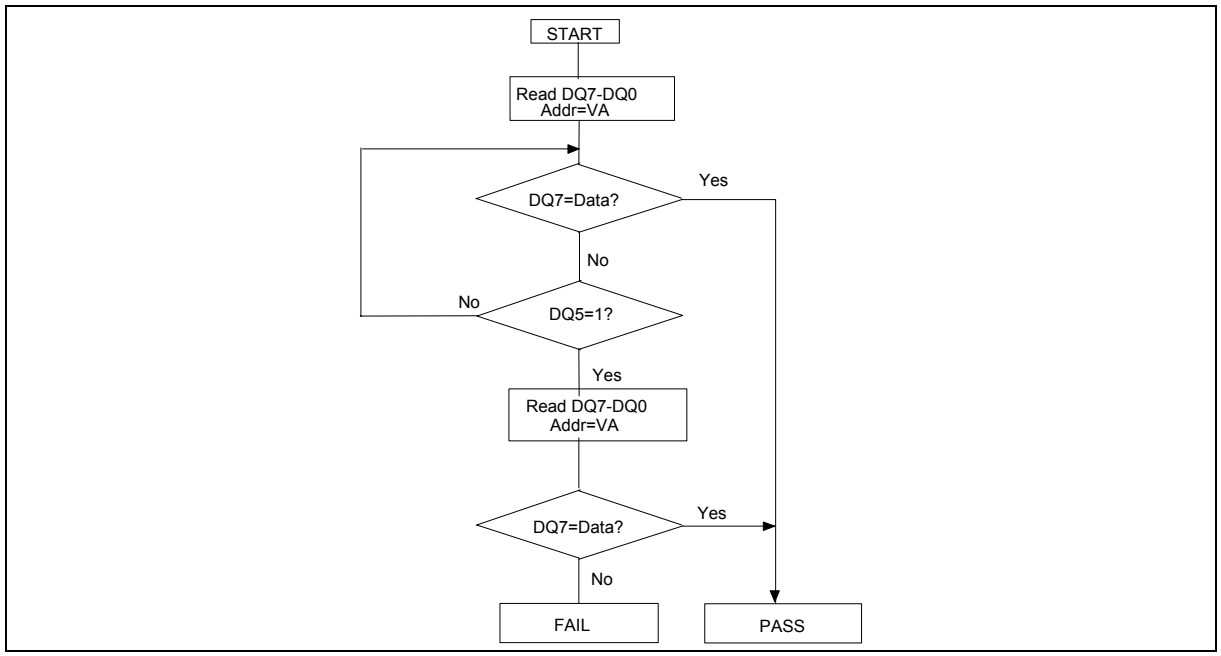
7.11 Erase Algorithm



Notes:

1. See Command Definitions Table for erase command sequence details.
2. See DQ3 section for the sector erase timer details.

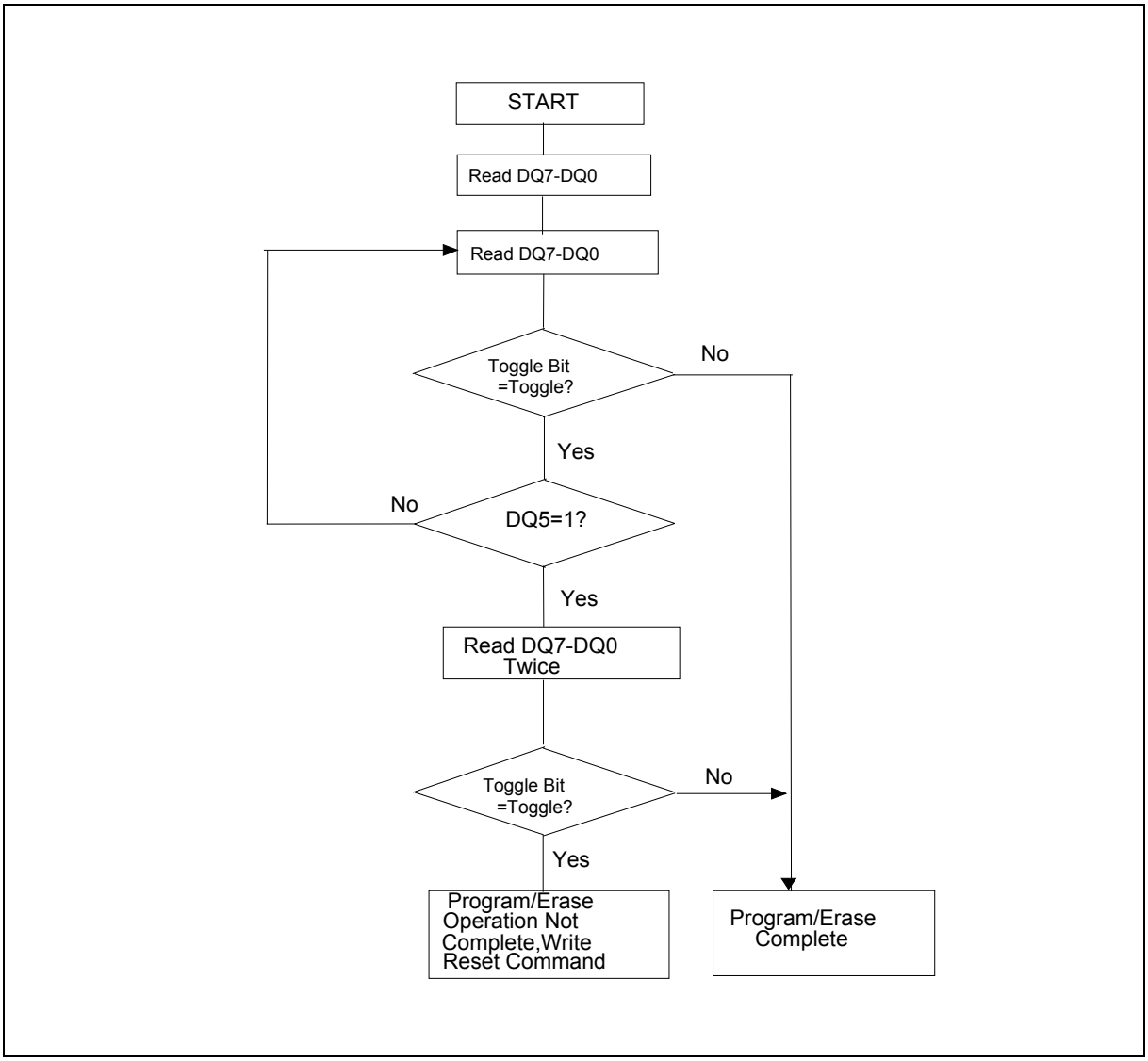
7.12 Data Polling Algorithm



Notes:

1. VA = Valid address for programming. During a sector erase operation; a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
2. DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.

7.13 Toggle Bit Algorithm



Note: The system should recheck the toggle bit even if DQ5 ="1" because the toggle bit may stop toggling as DQ5 changes to "1". See DQ6 and DQ2 section for more information

8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

PARAMETER		RATING	UNIT
Storage Temperature Plastic Packages		-65 to +150	°C
Ambient Temperature with Power Applied		-65 to +125	°C
Voltage with Respect to Ground	V_{DD} (Note 1)	-0.5 to +4.0	V
	A9, #OE, and #RESET (Note 2)	-0.5 to +11.5	V
	#WP/ACC	-0.5 to +10.5	V
	All other pins (Note 1)	-0.5 to V_{DD} +0.5	V
Output Short Circuit Current (Note 3)		200	mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{DD} +0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{DD} +2.0 V for periods up to 20 ns.
2. Minimum DC input voltage on pins A9, #OE, #RESET, and #WP/ACC is -0.5 V. During voltage transitions, A9, #OE, #WP/ACC, and #RESET may overshoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on pin A9 is +11.5 V which may overshoot to +14.0 V for periods up to 20 ns. Maximum DC input voltage on #WP/ACC is +9.5 V which may overshoot to +12.0 V for periods up to 20 ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

8.2 Operating Ranges

PARAMETER		RATING	UNIT
Ambient Temperature (TA)	Industrial Grade	-40 to +85	°C
	Extended Grade	-20 to +85	
V_{DD} Supply Voltages V_{DD} for standard voltage range		2.7 to 3.6	V

Operating ranges define those limits between which the functionality of the device is guaranteed.

8.3 DC Characteristics

8.4 CMOS Compatible

PARAMETER	SYM.	TEST CONDITIONS		LIMITS			UNIT
				MIN.	TYP.	MAX.	
Input Load Current	I_{LI}	V_{IN} =V_{SS} to V_{DD}, V_{DD} = V_{DD} (Max.)		-	-	±1.0	µA
A9 Input Load Current	I_{LIT}	V_{DD} = V_{DD} (Max.), A9 = V_{ID} (Max.)		-	-	35	µA
Output Leakage Current	I_{LO}	V_{OUT} =V_{SS} to V_{DD}, V_{DD} =V_{DD} (Max.)		-	-	±1.0	µA
V_{DD} Active Read Current (Note 1, 2)	I_{CC1}	#CE = V_{IL}, #OE = V_{IH} Byte Mode	5 MHz	-	10	16	mA
			1 MHz		2	4	mA
		#CE = V_{IL}, #OE = V_{IH} Word Mode	5 MHz		10	16	mA
			1 MHz		2	4	mA
V_{DD} Active Write Current (Note 2, 3)	I_{CC2}	#CE = V_{IL}, #OE = V_{IH}, #WE = V_{IL}		-	15	30	mA
V_{DD} Standby Current (Note2,5)	I_{CC3}	#CE = V_{DD} ±0.3V, #RESET = V_{DD} ±0.3V		-	0.2	5	µA
V_{DD} Reset Current (Note2)	I_{CC4}	#RESET = V_{SS} ±0.3V		-	0.2	5	µA
Automatic Sleep Mode Current (note 2, 4,5)	I_{CC5}	V_{IH} = V_{DD} ±0.3V, V_{IL} = V_{SS} ±0.3V		-	0.2	5	µA
V_{DD} Active Program-While-Erase-Suspended Current (note 2, 6)	I_{CC6}	#CE = V_{IL}, #OE = V_{IH}		-	17	35	mA
ACC Accelerated Program Current, Word or Byte	I_{Acc}	#CE = V_{IL}, #OE = V_{IH}	ACC Pin		5	10	mA
			VDD Pin		15	30	mA
Input Low Voltage	V_{IL}	-		-0.5	-	0.8	V
Input High Voltage	V_{IH}	-		0.7x V_{DD}	-	V_{DD} +0.3	V
Voltage for #WP/ACC Sector Protect/ Unprotect and Program Acceleration	V_{HH}	V_{DD} =3.0V ±10%		8.5	-	9.5	V
Voltage for AUTOSELECT and Temporary Sector Unprotected	V_{ID}	V_{DD} =3.0V ±10%		8.5	-	11.5	V
Output Low Voltage	V_{OL}	I_{OL} = 4.0 mA, V_{DD} = V_{DD} (Min.)		-	-	0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.0 mA, V_{DD} = V_{DD} (Min.)		0.85 V_{DD}	-	-	V
	V_{OH2}	I_{OH} = -100 µA, V_{DD} = V_{DD} (Min.)		V_{DD} -0.4	-	-	

Notes:

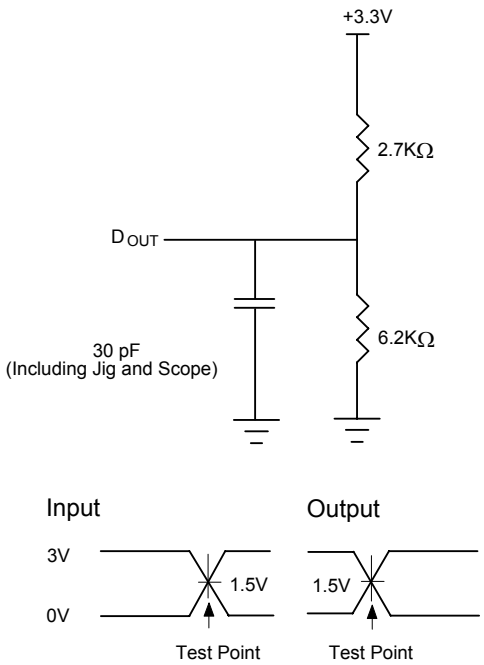
1. The I_{CC} current listed is typically less than 2 mA/ MHz, with #OE at V_{IH}.
2. Maximum I_{CC} specifications are tested with V_{DD} = V_{DD} max.
3. I_{CC} active while Embedded Erase or Embedded Program is in progress.
4. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is200 nA.
5. For temperature >70 degree C, Vih(Max.)=Vdd+0.1V and Vil(Min)=Vss-0.1V.
6. Not 100% tested

8.5 AC Characteristics

8.6 Test Condition

TEST CONDITION	70ns	UNIT
Output Load	1 TTL gate	
Output Load Capacitance, CL (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0-3.0	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V

8.6.1 AC Test Load and Waveforms



8.7 Read-Only Operations

PARAMETER		SYM.	TEST SETUP	70ns		UNIT
				MIN.	MAX.	
Read Cycle Time		TRC		70	-	ns
Address to Output Delay		TACC	#OE, #CE =VIL	-	70	ns
Chip Enable to Output Delay		TCE	#OE, = VIL	-	70	ns
Output Enable to Output Delay		TOE		-	30	ns
Chip Enable to Output High Z		TDF		-	16	ns
Output Enable to Output High Z		TDF		-	16	ns
Output Hold Time From Address, #OE or #CE, Whichever Occurs First		TOH		0	-	ns
Output Enable Hold Time	Read	TOEH		0	-	ns
	Toggle and #Data polling			10	-	ns

Note: Not 100 % tested

8.8 Hardware Reset (#RESET)

PARAMETER	SYM.	MIN.	MAX.	UNIT
#RESET PIN Low (During Embedded Algorithms) to Read Mode	TReady	-	20	μs
#RESET Pin Low (Not During Embedded Algorithms) to Read Mode	TReady	-	500	ns
#RESET Pulse Width	TRP	500	-	ns
Reset High Time Before Read	TRH	50	-	ns
#RESET Low to Standby Mode	TRPD	20	-	μs
RY/#BY Recovery Time	TRB	0	-	ns

Note: Not 100 % tested

8.9 Word/Byte Configuration (#BYTE)

PARAMETER	SYM.	70ns		UNIT
		MIN.	MAX.	
#CE to #BYTE Switching Low or High	TELFL/TELFH	-	5	ns
#BYTE Switching Low to Output High Z	TFLQZ	-	16	ns
#BYTE Switching High to Output Active	TFHQV	70	-	ns

8.10 Erase and Program Operation

PARAMETER		SYM.	70ns			UNIT
			MIN.	TYP.	MAX.	
Write Cycle Timing (Note 1)		TWC	70	-	-	ns
Address setup Time		TAS	0	-	-	ns
Address Setup Timing to #OE low during toggle bit polling		TASO	15	-	-	ns
Address Hold Time		TAH	45	-	-	ns
Address Hold Time From #CE or #OE high during toggle bit polling		TAHT	0	-	-	ns
Data Setup Time		TDS	35	-	-	ns
Data Hold Time		TDH	0	-	-	ns
Output Enable High During toggle bit polling		TOEPH	20	-	-	ns
Read Recovery Time Before Write (#OE High to #WE Low)		TGHWL	0	-	-	ns
#CE Setup Time		TCS	0	-	-	ns
#CE HOLD Time		TCH	0	-	-	ns
Write Pulse Width		TWP	30	-	-	ns
Write Pulse Width High		TWPH	30	-	-	ns
Latency Between Read and Write Operation		TSR/W	0	-	-	ns
Programming Time (Note 2)	Byte	TPB	-	7	150	µs
	Word	TPW	-	9	210	µs
Accelerated Programming Time (Noe2)	Byte	TACCP	4		-	µs
	Word					
Sector Erase Time (Note 2)		TSE	-	0.4	-	sec
VDD Setup Time (Note 1)		TVCS	50	-	-	µs
Write Recovery Time from RY/#BY		TRB	0	-	-	ns
Program/Erase Valid to RY/#BY Delay		TBUSY	90	-	-	ns

Notes:

1. Not 100 % tested
2. See the "Alternate #CE Controlled Erase and Program Operations" section for more information

8.11 Temporary Sector Unprotect

PARAMETER	SYM.	MIN.	MAX.	UNIT
VID Rise and Fall Time	TVIDR	500	-	ns
VHH Rise and Fall Time	TVHH	250	-	ns
#RESET Setup Time for Temporary Sector Unprotect	TRSP	4	-	µs
#RESET Hold Time from RY/#BY High for Temporary Sector Unprotect	TRRB	4	-	µs

Note: Not 100 % tested

8.12 Alternate #CE Controlled Erase and Program Operations

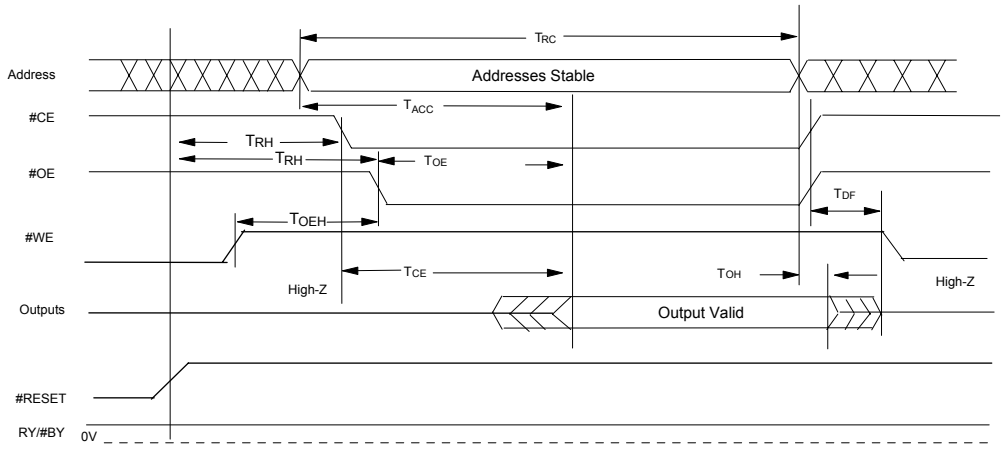
PARAMETER		SYM.	70 ns			Unit
			Min.	Typical (Note3)	Max. (Note4)	
Write Cycle Time (Note 1)		TWC	70	-	-	ns
Address Setup Time		TAS	0	-	-	ns
Address Hold Time		TAH	45	-	-	ns
Data Setup Time		TDS	35	-	-	ns
Data Hold Time		TDH	0	-	-	ns
Read Recover Time Before Write (#OE High to #WE Low)		TGHEL	0	-	-	ns
#WE Setup Time		TWS	0	-	-	ns
#WE Hold Time		TWH	0	-	-	ns
#CE Pulse Width		TCP	30	-	-	ns
#CE Pulse Width High		TCPH	30	-	-	ns
Programming Time (Note 6)	Byte	TPB	-	7	150	µs
	Word	TPW	-	9	210	
Accelerated Programming Time (Note 6)	Byte	TACCP	-	4	120	µs
	Word					
Sector Erase Time (Note 2)		TSE	-	0.4	15	sec
Chip Erase Time (Note 2)		TCE	-	30	-	sec
Chip Program Time (Note 5)	Byte	TCPB	-	21	63	sec
	Word	TCPW	-	14	42	

Notes:

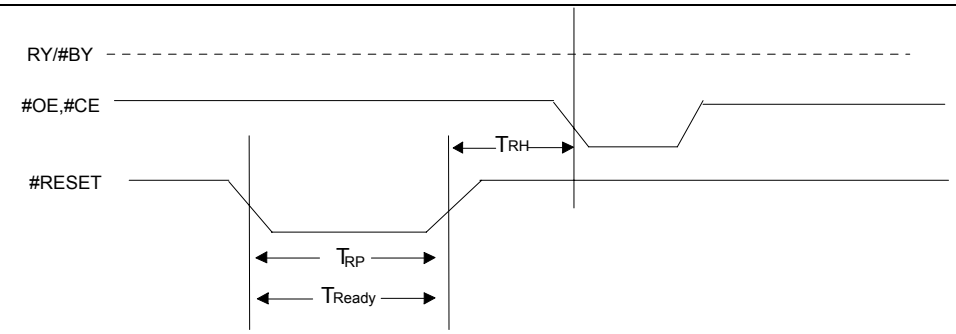
1. Not 100 % tested.
2. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
3. Typical program and erase time assume the following conditions :25℃,3.0 V V_{DD}, 100,000 cycles .Additionally, programming typicals assume checkerboard pattern.
4. Under worst case conditions of 90℃, V_{DD} =2.7V, 100,000 cycles.
5. The typical chip programming time is considerably less than the maximun chip programming time listed,since most bytes program faster than maximun program times listed.
6. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command.
7. The device has a minimum erase and program cycle endurance of 100,000 cycles.

9. TIMING WAVEFORMS

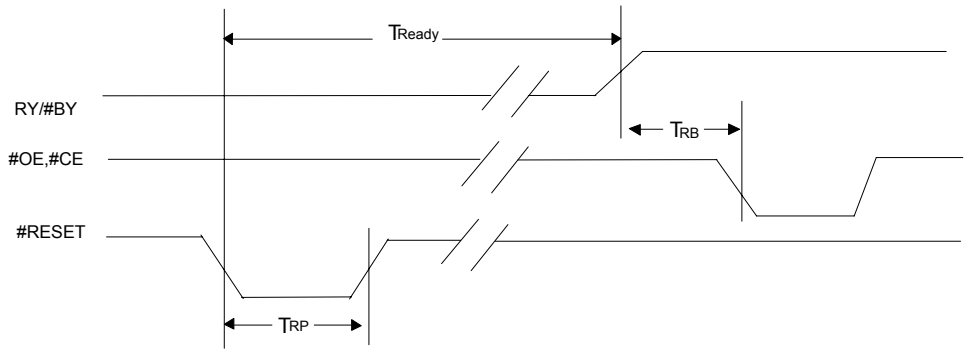
9.1 AC Read Waveform



9.2 Reset Waveform

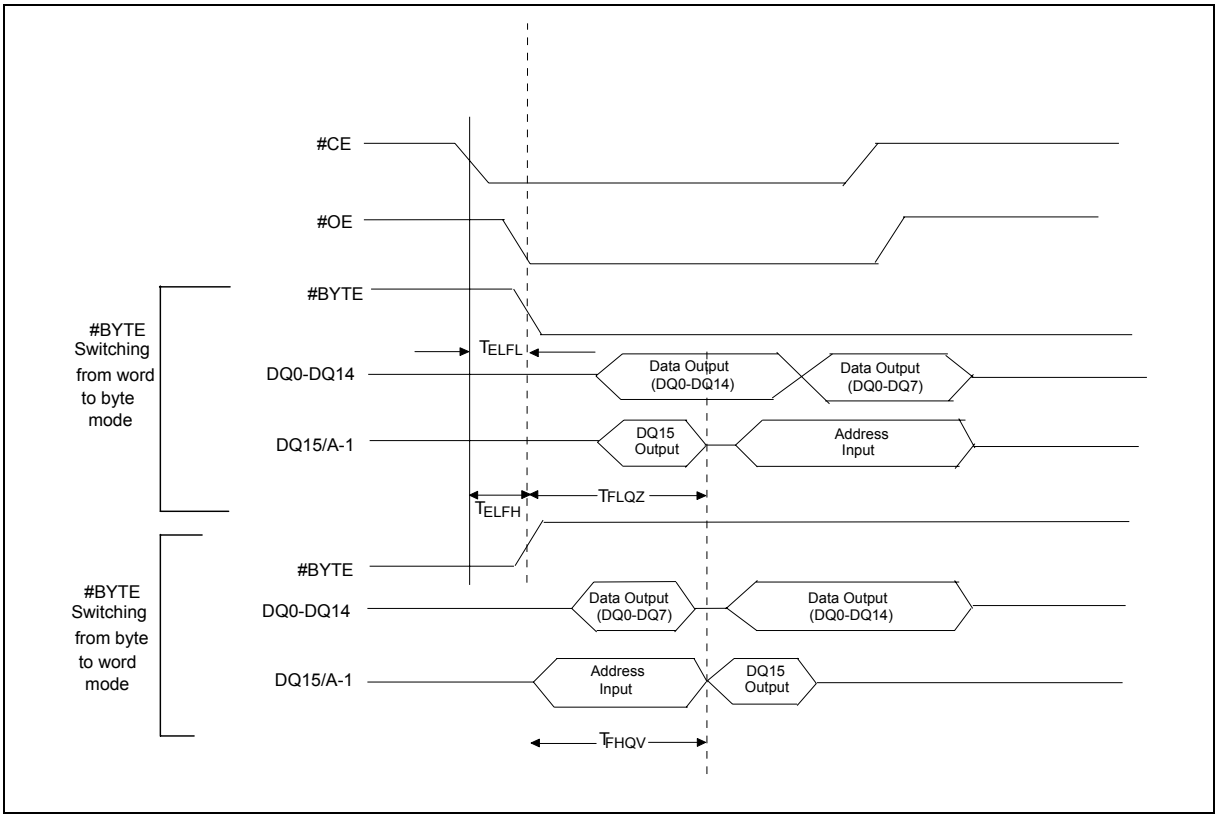


Reset Timing NOT during Embedded Algorithms

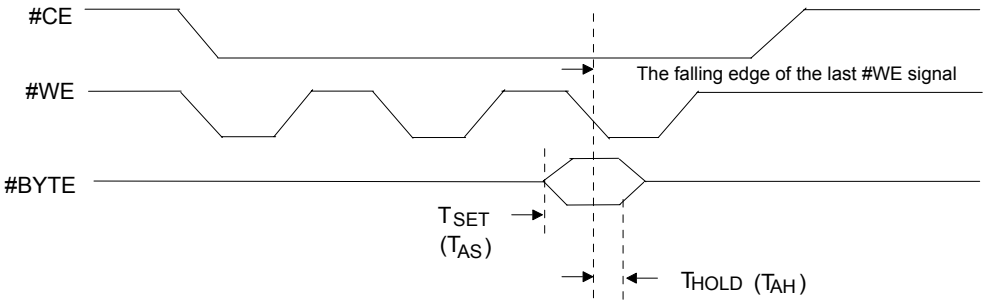


Reset Timings during Embedded Algorithms

9.3 #BYTE Waveform for Read Operation

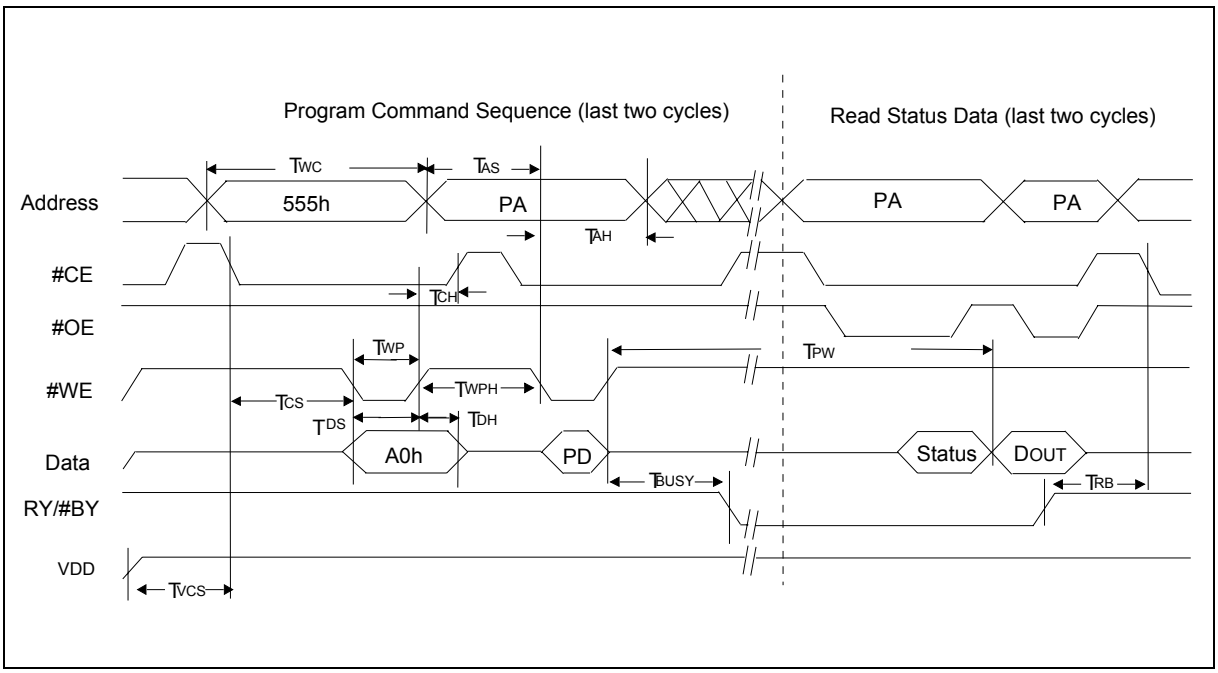


9.4 #BYTE Waveform for Write Operation



Note: Refer to the Erase /Program Operations table for TAS and TAH Specifications.

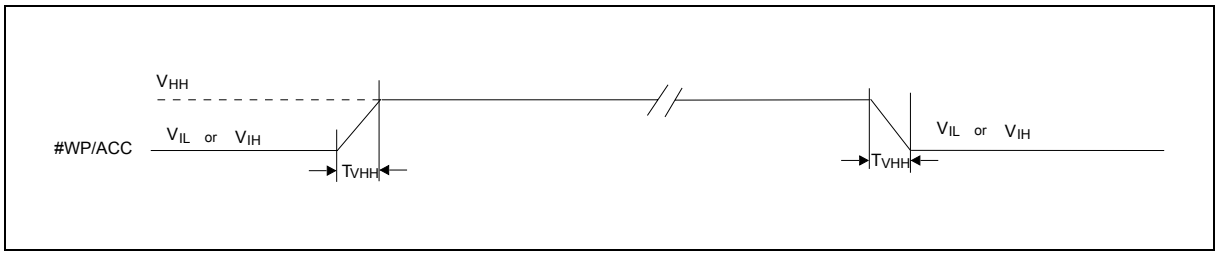
9.5 Programming Waveform



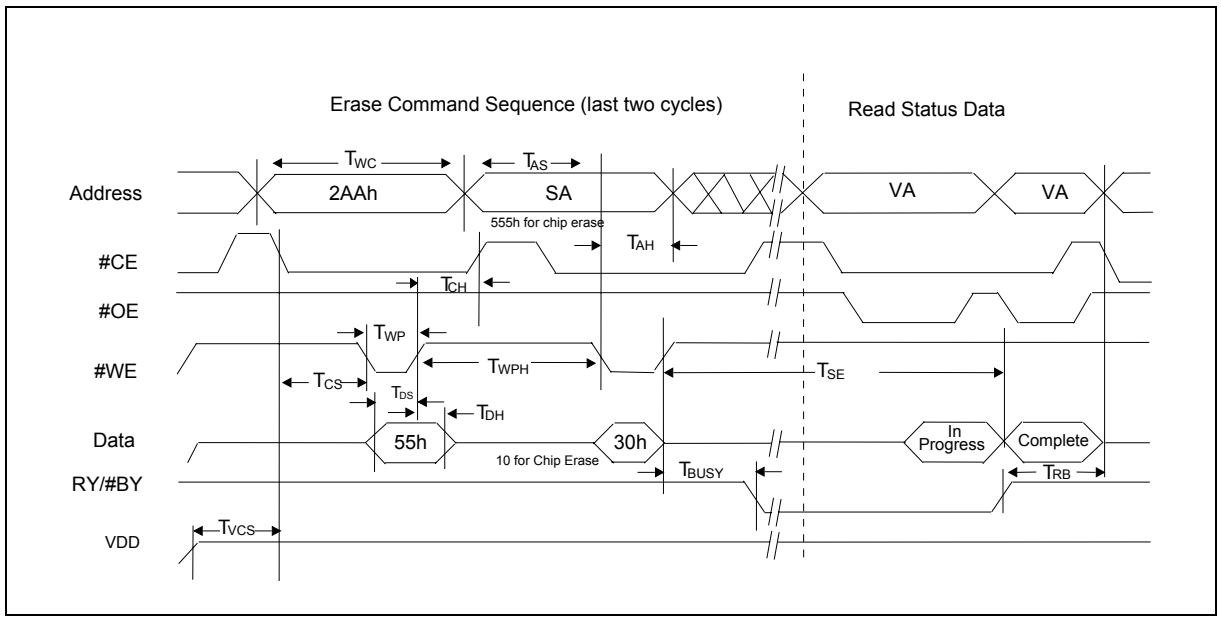
Notes:

1. PA = program address, PD = program data,DOUT is the true data at the program address
2. Illustration shows device in word mode

9.6 Accelerated Programming Waveform



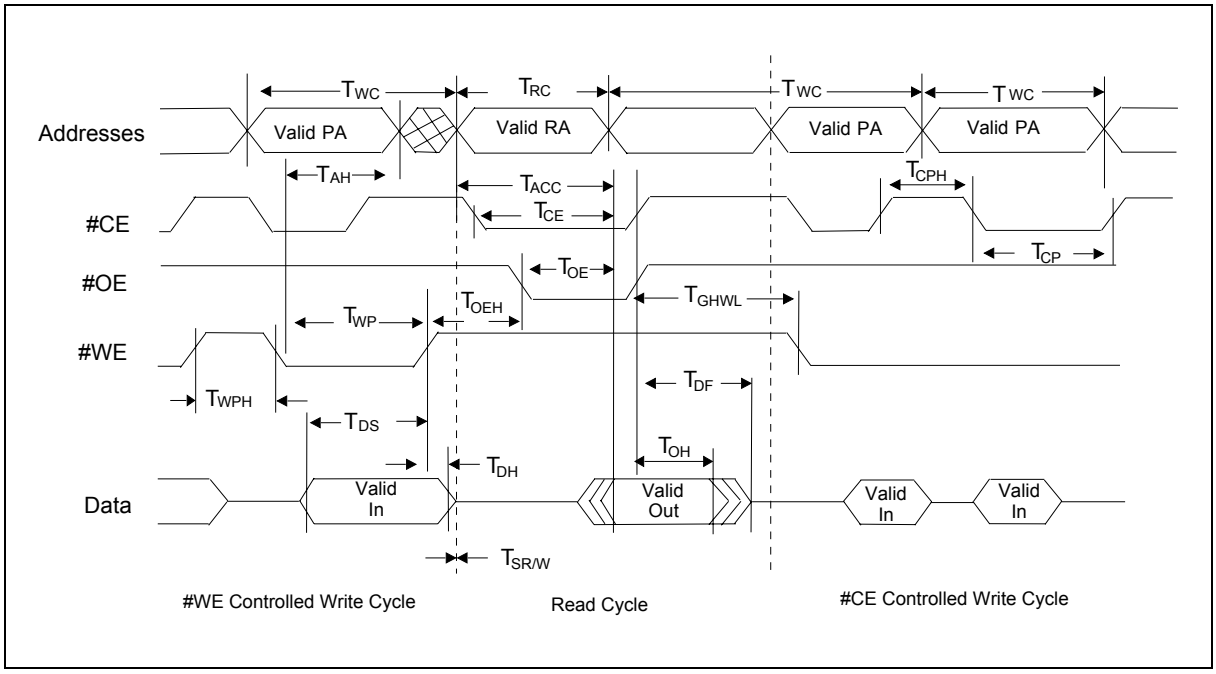
9.7 Chip/Sector Erase Waveform



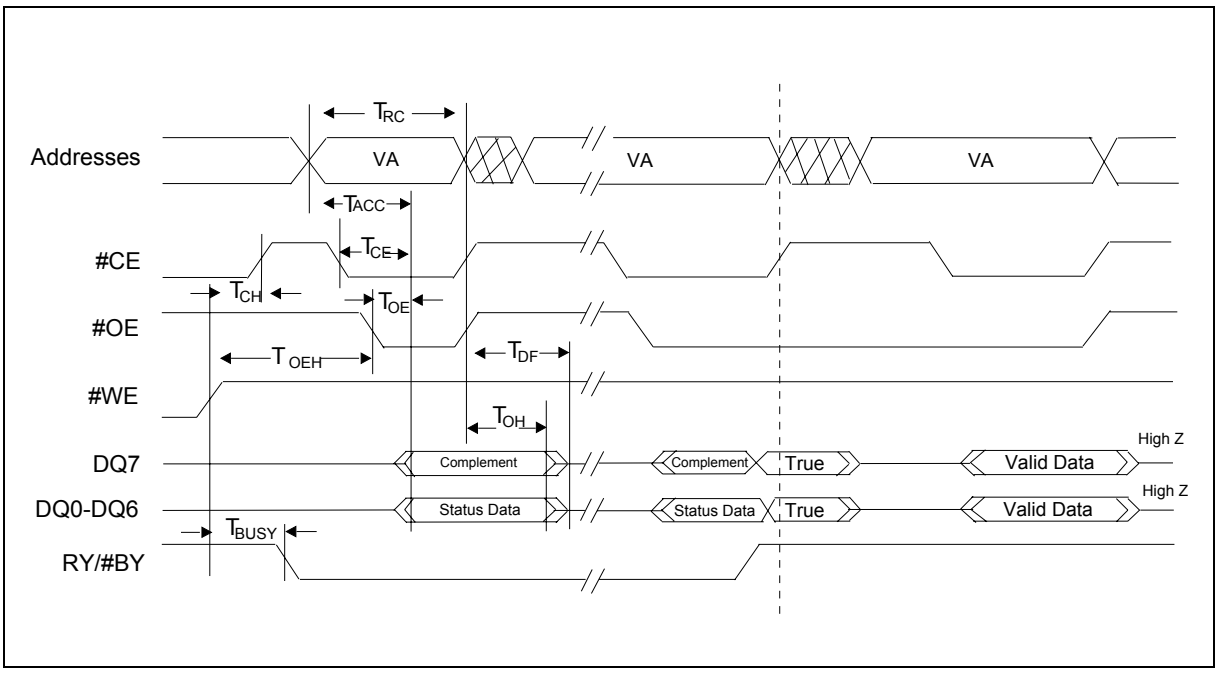
Notes :

1. SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see “Write operation Status”).
2. These waveforms are for the word mode

9.8 Back-to back Read/Write Cycle Waveform

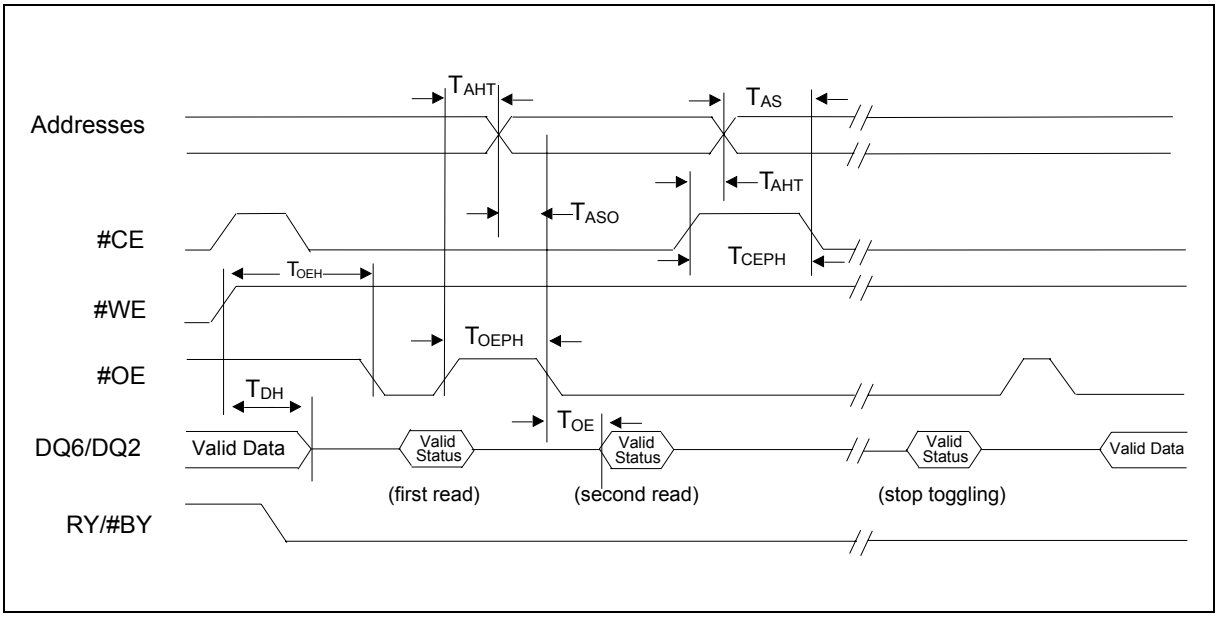


9.9 #Data Polling Waveform (During Embedded Algorithms)



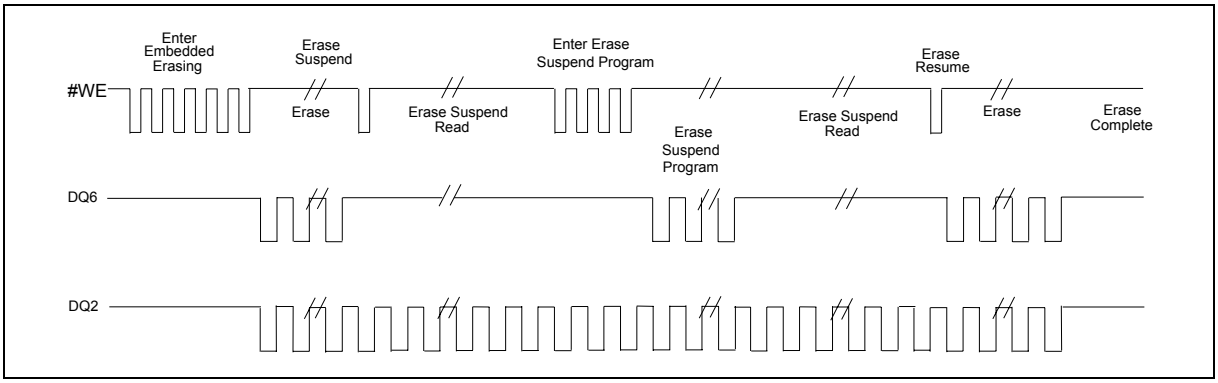
Note: VA= Valid Address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

9.10 Toggle Bit Waveform (During Embedded Algorithms)



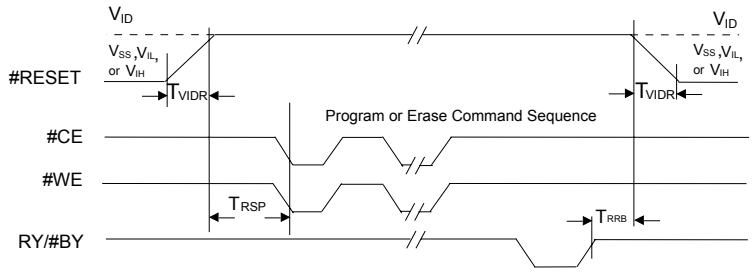
Note: VA= Valid address;not requires for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

9.11 DQ 2 vs. DQ6 Waveform

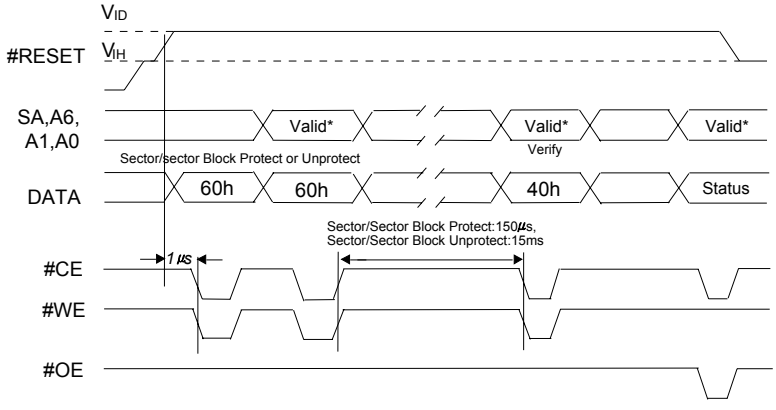


Note: DQ2 toggles only when read at an address within an erase-suspended sector. The sysytem may use #OE or #CE to toggle DQ2 and DQ6.

9.12 Temporary Sector Unprotect Timing Diagram

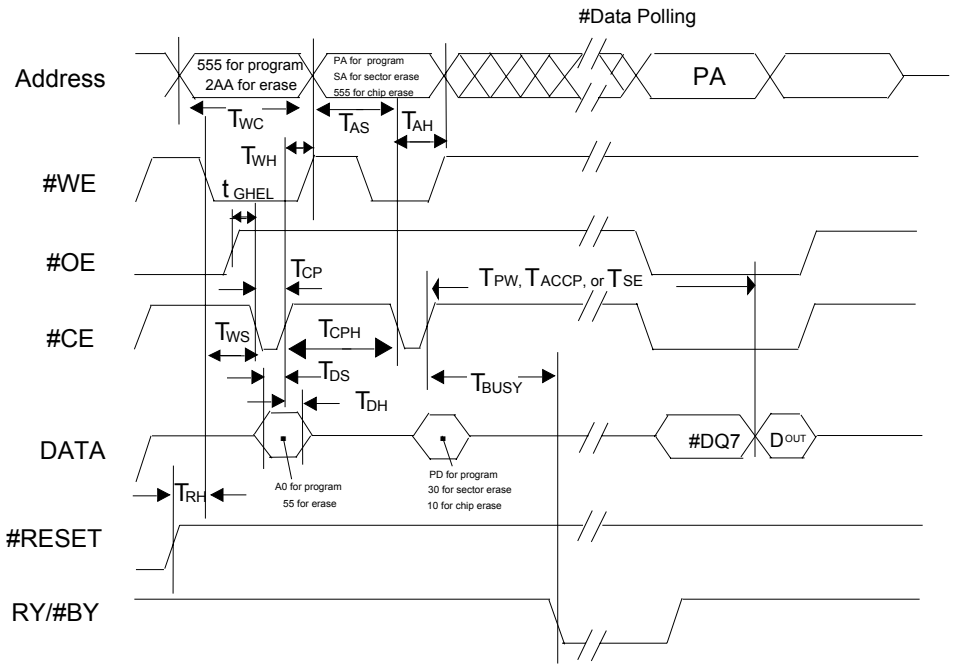


9.13 Sector/Sector Block Protect and Unprotect Timing Diagram



**For sector protect,A6=0,A1=1,A0=0.For sector unprotect ,A6=1,A1=1,A0=0*

9.14 Alternate #CE Controlled Write (Erase/Program) Operation Timing



Notes:

1. Firgure indicates last two bus cycles of a program or erase operation.
2. PA= program address, SA= sector address, PD= program data.
3. #DQ7 is the complement of the data written to the device. Dout is the data written to the device.
4. Waveforms are for the word mode.

10. LATCHUP CHARACTERISTICS

PARAMETER	MIN.	MAX.
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, #OE, and #RESET)	-1.0V	11.5 V
Input voltage with respect to V_{SS} on all I/O pins	-1.0V	V_{DD} +1.0V
V_{DD} Current	-100mA	+100mA

Note: Includes all pins except V_{DD}. Test conditions: V_{DD} = 3.0 V, one pin at a time.

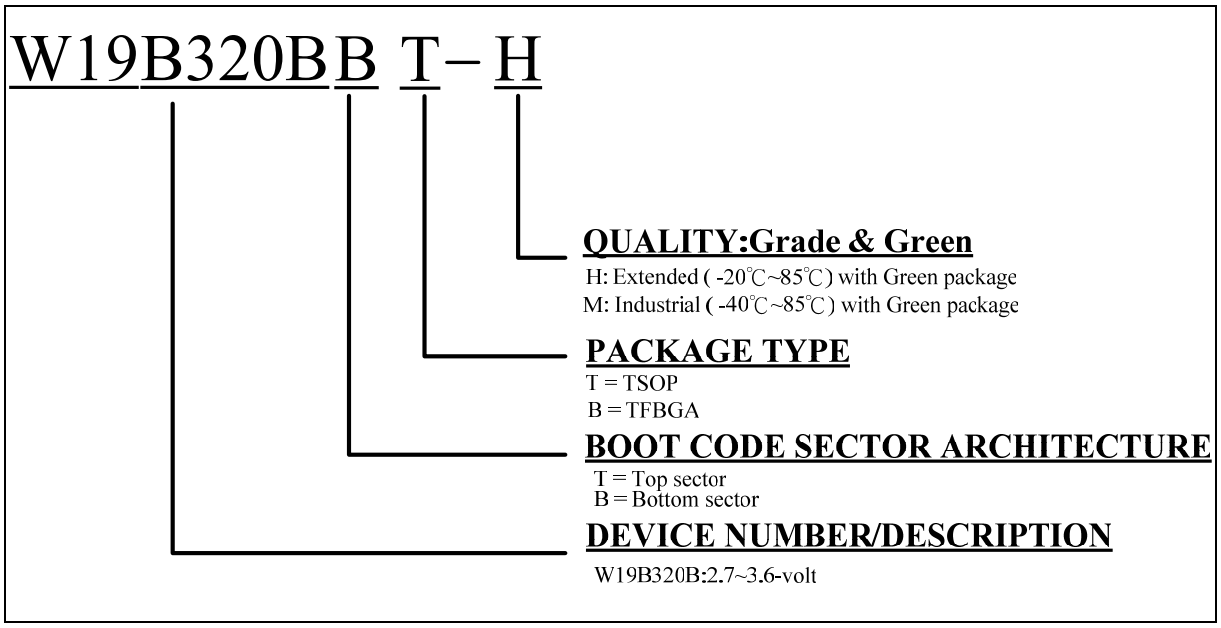
11. CAPACITANCE

PARAMETER	SYM.	TEST SETUP	TSOP		TFBGA		UNIT
			Typical	Max.	Typical	Max.	
Input Capacitance	CIN	VIN = 0	6	7.5	4.2	5.0	pF
Output Capacitance	COUT	VOUT = 0	8.5	12	5.4	6.5	pF
Control Pin Capacitance	CIN2	VIN = 0	7.5	9	3.9	4.7	pF

Notes:

1. Sampled, not 100 % tested.
2. Test condition TA = 25 °C, f = 1.0 MHz.

12. ORDERING INFORMATION

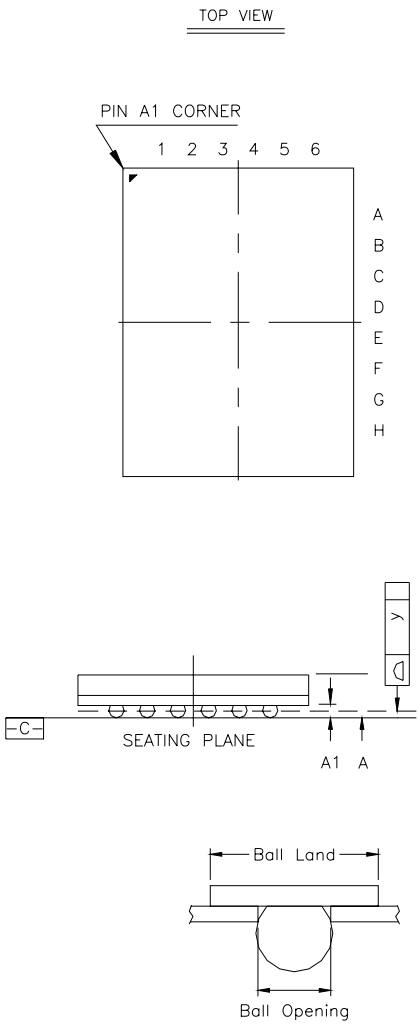


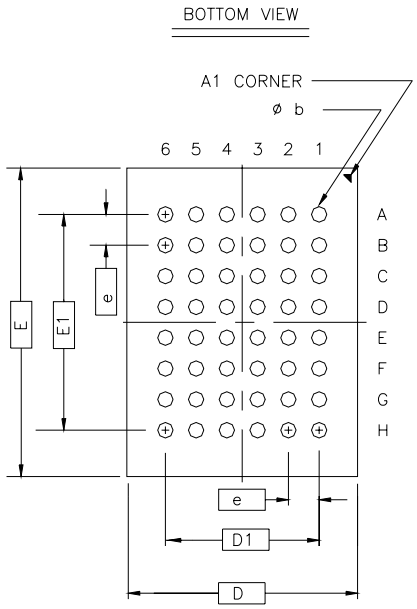
Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

13. PACKAGE DIMENSIONS

13.1 TFBGA48ball (6X8 mm^2, Ø=0.40mm)



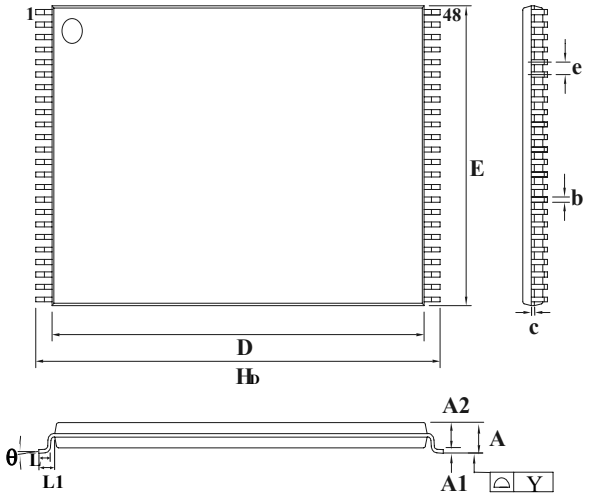


Controlling Dimension :Millimeters

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	–	–	1.20	–	–	0.0472
A1	0.27	–	0.37	0.0106	–	0.0146
D	6.00			0.2362		
D1	4.00 REF.			0.1575 REF.		
E	8.00			0.3149		
E1	5.60 REF.			0.2204 REF.		
y	0.12 REF.			0.0047 REF.		
øb	0.38	–	0.48	0.0149	–	0.0188
e	–	0.80	–	–	0.0315	–

Note: Ball Land: 0.50mm / Ball opening: 0.35mm

13.2 48-Pin Standard Thin Small Outline Package



Sym.	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	—	0.002	—	—
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	18.3	18.4	18.5	0.720	0.724	0.728
H_D	19.8	20.0	20.2	0.780	0.787	0.795
E	11.9	12.0	12.1	0.468	0.472	0.476
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.10	—	0.21	0.004	—	0.008
e	—	0.50	—	—	0.020	—
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	—	0.80	—	—	0.031	—
Y	—	—	0.10	—	—	0.004
θ	0	—	5	0	—	5

14. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A0	Dec,31, 2006	ALL	Initial Issued ,note p21
A1	June,15,2007	ALL	1. VID was changed from 12.5 to 11.5 2. Erase time was changed form 49 Sec to 30Sec 3. Re-typesetting
A2	Oct,17,2007	46	Update package material as Green
A3	Dec.25,2007	41,44,45	1. Add note 5 and 6 2. Add max of tPB and tPW 3. Modify format and setting

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